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| High Speed Switch |
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**Abstract:**

Fair queuing is a technique that allows each flow passing through a network device to have fair share of network resources. Previous schemes for fair queuing that achieved nearly perfect fairness were expensive to implement; specifically, the complexity to process a packet in these schemes was O(, where is the number of active flows. This is expensive at high speeds.

We have developed a lightweight Deficit Round Robin scheduler for the input arbiter of the NetFPGA router. The NetFPGA is an open networking platform accelerator that enables rapid development of hardware-accelerated packet processing applications. Our scheme achieves nearly perfect fairness in terms of throughput.

The design is effective in reducing latency for small packets from one port in the presence of saturating traffic of large packets from another port. The design hides arbitration latency when multiple channels are active and achieves nearly optimal latency for the NetFPGA architecture. The design demonstrates that lightweight Fair Queuing algorithms can be useful for simple arbitration without introducing an additional queuing stage which increase both complexity and latency.

We evaluate the Deficit Round Robin Input Arbiter in four ways

* Running two testbenches comparing both RR and DRR Input Arbiter’s. We inject random packets size to each FIFO and plot throughput versus average packet size.
* Measuring Fairness Index / throughput versus quantum, with scenario that certain queues always have large packets size & other queues have random size with average less than large packets size.
* Measuring delay of both RR & DRR given that one queue is injected by small packets size & the second queue is injected by large packets size.
* Measuring throughput of DRR, when connecting the first NetFPGA port with the second port.

**CONCLUSION:**

This DRR scheduler for the input arbiter of the NetFPGA demonstrates that fair scheduling properties can be achieved with less complexity to current design of RR Input Arbiter. DRR should be at attractive to use while implementing Fair Queuing at gateways and routers. They should be useful in networks where each port represent single machine as it provides isolation property. Also DRR prevent rouge users from exhausting resources.

We have described DRR scheme that provides near-perfect isolation at very low implementation cost.As far as we know, this is the first fair queuing solution that provides near-perfect throughput fairness with o (1) packet processing.

We have illustrated that DRR behaves fair as shown in simulation results; also we describe the behavior of DRR in ensuring throughput fairness versus RR technique. From our results we concluded the suitable quantum value that provides the approximated fairness & a low maximum throughput.

DRR can be applied to other scheduling techniques contexts in which jobs must be serviced as whole units, such as token ring with holding timers & load balancing. For these reasons, we believe that DRR scheduling in a general and useful tool.