Fully-Integrated Frequency-Hopping Manpack Transceiver

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1st Quarter Report

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Executive Summary

Manpack devices are one of the important modules that are used in different military situations. Frequency hopping has been the main modulation scheme that is used in such devices due to the benefits it provides for security purposes. The first Egyptian Frequency Hopping Manpack system was developed in our department in collaboration with the Egyptian military. The system was designed and assembled using commercial components on printed circuits boards.

The prototype has been sampled, and field tested and is going through a first production phase. This prototype has a few drawbacks that need to be addressed for future generations. Size, weight, power consumption, frequency ranges and hopping rate are among these issues. In this proposal, we are planning to implement enhancements to this system in order to provide solutions for these issues that can serve as the core of the second generation Frequency Hopping Manpack System.

This proposal focuses only on the transceiver side and its implementation. New specifications include frequency range of 30MHz-500MHz and hopping rate of 300 hop/sec. In this proposal, a fully integrated transceiver is planned to improve the system from all aspects. On-chip integration reduces the size drastically and in case of mass production, cost per unit also reduces dramatically. On-chip techniques provide solutions for many problems and provide innovative techniques that are mostly not possible in the discrete-component implementation.

In this proposal we are targeting a 10x reduction in cost for mass production, which is not possible in the first prototype since all components are off the shelf and their cost cannot be reduced unless they are combined together or integrated as is the case in this work. This proposal describes the issues facing the current solution and proposes solutions on different levels of the design. Power consumption reduction is based on improving the power amplifier's power efficiency as well as improving reflection behavior with the antenna on both directions. A power reduction of 5x is targeted.

This is a challenging task but achievable by changing the power amplifier architecture and customizing it to the system's need. Widening the frequency range (30MHz-500MHz) in this proposal compared to the original design poses more challenges to the circuit design. Hence, a new architecture has been introduced in this proposal that relaxes the different block-level specifications. Extensive programmability is used. Frequency planning is modified to accommodate for the new frequency requirements and at the same time to optimize the total power consumption as well as the complexity of the circuit design.

List of Deliverables

Table 1: List of deliverables

Month # 6	System Level Architecture Design with all required block specifications and intial circuit architectures with preliminary results.
Month # 12	Circuit level architectures, design and transistor-level simulations of all blocks. Report will include corner simulations under different design conditions (Supply variations, temperature variations, device models ... etc).
Month # 18	Top-level simulations, Chip Floorplan, block-Level Layout, Top-level layout, post-layout simulations and GDS of the sent chip.
Month # 24	Final System Measurement Results of the fully integrated transceiver. The report will be showing the results obtained from the bench testing and comparison with the simulations expectations and Final Report.

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Part I
System Level Design

1 INTRODUCTION TO RECEIVER ARCHITECTURES

1.1 Direct Conversion (Homodyne)

Homodyne comes from the Latin words: HOMO, which means same, and DYNE, which means mixing. A homodyne receiver uses a local oscillator which has the same frequency as the carrier frequency hence translating the signal to DC. For the down-conversion of an asymmetrically modulated signal to a zero center frequency leads to signal self corruption, quadrature mixing is required for direct conversion radios. A typical homodyne receiver is shown in Figure 1.

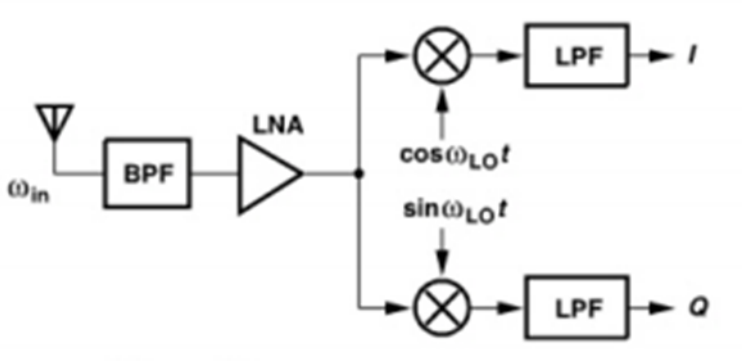

Figure 1: Direct Conversion Receiver

1.1.1 Homodyne Receiver Impairments

Homodyne offers great integration capabilities for radio receivers; however, several issues arise that need be addressed when designing a homodyne radio.

LO Leakage Homodyne receivers emit a fraction of their LO power from their antenna, leakage could be due to substrate coupling or backward propagation from the LO Port through the RF Port to the LNA input. Such leakage acts as an interferer and may desensitize nearby receivers. LO leakage can be minimized through symmetric layout of the local oscillator and the RF signal path.

DC offsets Time Varying DC offsets maybe caused by self mixing. The LO leak at the RF port mixes itself to a DC component that gets amplified throughout the RF path. Such an offset may grow in amplitude that it could saturate baseband blocks (VGAs or ADCs). DC offsets could be minimized using either high pass filtering (corrupting the signal) or DC offset cancellation loops (foreground and background DC Offset Cancellation "DCOC").

Even Order Distortion While third order inter-modulation products result in desensitization and compression, second order inter-modulation products that are near DC do corrupt the signal in direct conversion radios (DCRs). Implying a high constraint on the LNA IIP2 and the Mixer's RF to IF feed-through.

Flicker Noise Flicker noise, also known as 1/f noise, is a sort of noise in CMOS technology that is prevalent at low frequencies. Since DCRs convert the signal to be around DC, flicker noise does heavily corrupt the signal degrading the SNR calculated by only considering thermal noise. Flicker noise is characterized by the flicker frequency corner fc – Flicker noise penalty is calculated from the relationship $\frac{P_{n1}}{P_{n2}} = 1 + (5.9 + ln(\frac{f_c}{f_{BW}})).\frac{f_c}{f_{BW}}$ (Assuming channel bandwidth > Flicker corner frequency) where fBW is the channel bandwidth. For example; if a system's channel bandwidth is twice the Flicker noise corner frequency then, $P_{n1}/P_{n2} = 3.6$ and the system's noise figure is degraded by a whole 5.57 dB.

1.2 Heterodyne Receivers

The Heterodyne radio is a proven architecture; it has, until recently, been widely used in radio receivers. Heterodyne comes from the Latin words: HETERO, which means different, and DYNE, which means mixing. The signal is first translated to a lower intermediate frequency (IF) to relax the channel selection filter specifications, channel selection is carried out at the intermediate frequency and it can be achieved with an easier constraint on filter quality factor. An example of a heterodyne receiver is shown in Figure 2.

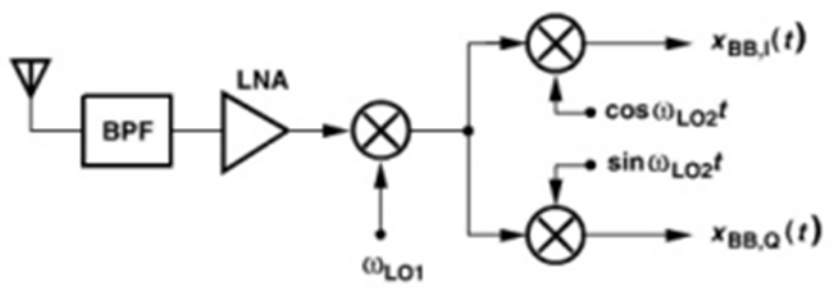

Figure 2: Heterodyne Receiver with quadrature down-conversion

1.2.1 Heterodyne Receiver Impairments

1.2.1.1 Mixing Spurs

For the LO signal is more of a square wave than a clean sinusoid, the LO can be expressed in the form: $P(t) = \frac{4}{\pi}[A_{LO}(cos(w_{LO}t) - \frac{1}{3}cos(3w_{LO}t) - \frac{1}{5}cos(5w_{LO}t) - \frac{1}{7}cos(7w_{LO}t)...]$. The LO odd harmonics would down-convert signals at (2n+1)FLO±FIF to the same band as the original signal. For high carrier frequencies, such harmonics would be suppressed by the band select filter. Mixing spurs become a major concern when dealing with wideband receivers where the LO harmonics lie in band and harmonic mixing would be a severe problem.

1.2.1.2 Thw Image Problem

The intermediate frequency translation gives rise to the image problem. As shown in Figure 3, for a signal centered at w_{RF} and assuming high side injection (w_{LO} *is at* $w_{RF} + w_{IF}$), the mixer would low-side-inject the signal residing at ($w_{IM} = w_{LO} + w_{IF} = w_{RF} + 2w_{IF}$). Such unwanted signal would severely corrupt the required information signal and hence needs be suppressed.

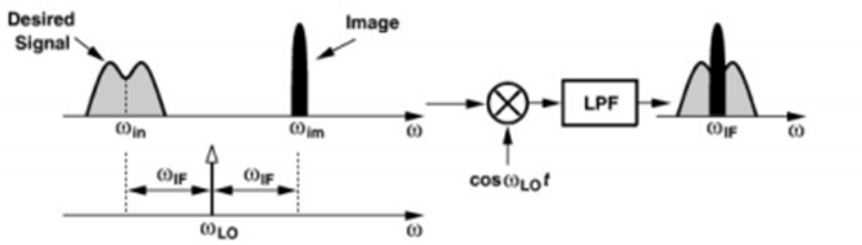

Figure 3: The Image Problem

The image band is suppressed by means of a very sharp off-chip Surface Acoustic Wave (SAW) filter. The selection of the Intermediate frequency is a trade-off between selectivity and sensitivity; as shown in Figure 4(a) when a high IF is chosen the image rejection ratio is high, but the channel select filter gets to operate at a higher center frequency giving less rejection to in-band interferers, hence degrading selectivity. Figure 4(b) shows that for a low IF, selectivity gets enhanced and channel select filter gets relaxed while sensitivity gets degraded due to low image rejection ratio.

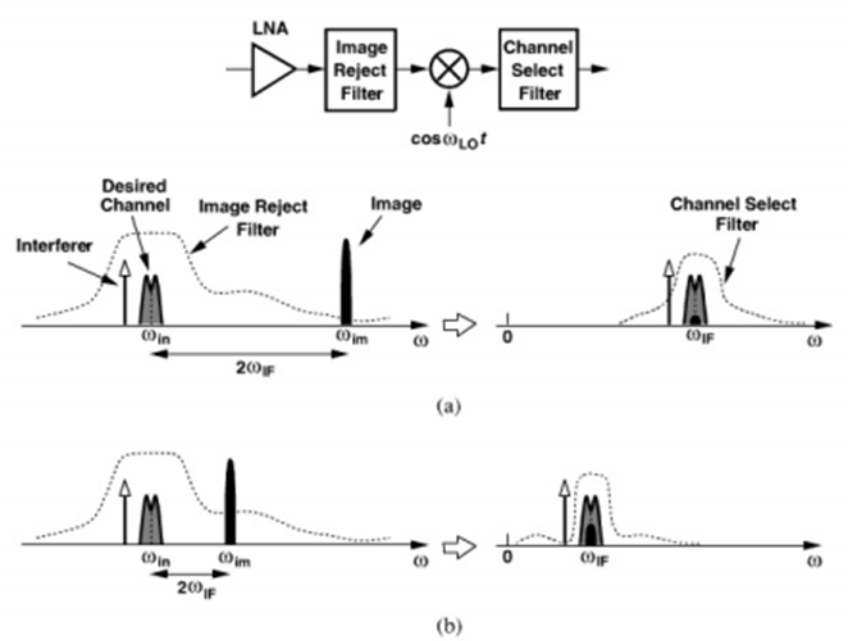

Figure 4: Trade-off between Image Rejection and Channel selection for (a) high IF and (b) low IF

1.2.2 Heterodyne Receiver Enhancements

Image Problem could be relaxed by solutions such as Dual IF; where the signal is first translated to a high IF hence enhancing image rejection (improving sensitivity), then the signal is translated to a low IF by means of a second mixing stage where channel selection could be easily carried out (improving selectivity). This gives rise to a problem that is referred to as the Secondary Image problem. The second mixing stage would have the signal at FIF1 and (assuming high side injection) a secondary image at (FIF1 + 2 FIF2). Such a problem could be solved by making the 2^{nd} IF at DC, (Zero-Second IF), comprising a radio architecture that has almost every impairment that exists in a direct conversion receiver.

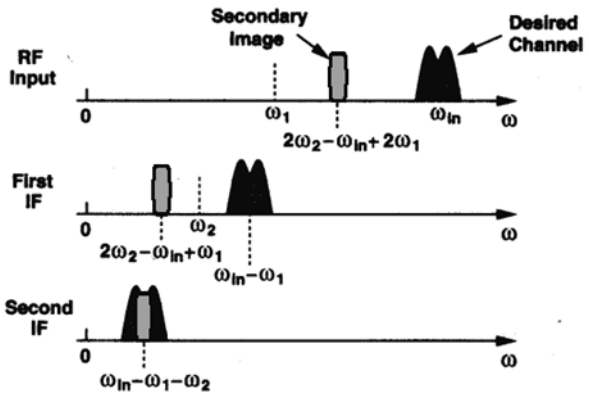

Figure 5: Secondary Image problem for Dual-IF Receivers

Such systems do not lend themselves well to integration, they have bulky off chip components, and consume a significant amount of power. Major modifications have been made for the basic heterodyne architecture in order to make it integration friendly and in order to try at solving its impairments without the need for bulky off-chip components.

1.2.3 Modern Heterodyne Receivers

1.2.3.1 Zero Second IF

A zero second IF eliminates the 2nd image problem by making the signal its own image. For a non symmetric signal zero second IF would lead to signal self corruption, hence quadrature mixing is required at the 2nd mixing stage.

1.2.3.2 Sliding IF

Sliding IF saves the architecture a Local Oscillator, using only one LO and by frequency division generates the second LO frequency. For a division ratio M and assuming zero second IF and low side injection at the first down-conversion, FRF=FLO + FLO/M. Hence FLO=M FRF/(M+1).

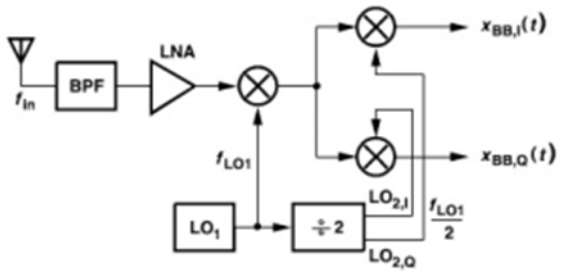

Figure 6: Divide by 2 Sliding IF Heterodyne Radio

One major challenge to Sliding IF radios stems from the need for a tunable filter to track the changing intermediate frequency. Draining more power and area but of course such a price is incomparable to the area and power required for a second LO.

1.2.4 Harmonic Rejection Techniques

Due to mixing spurs, unwanted signals at or around odd harmonics of the local oscillator are down-converted to IF, such signal do deteriorate signal to noise ratio (SNR) of the receiver.

Harmonic rejection allows for limiting the power of the unwanted IF signals. For narrow band systems, harmonic rejection can easily be implemented via the RF band select filter; such filters provide great attenuation for signals at odd harmonics of the local oscillator. Such techniques don't work out that well when the radio is wideband and the local oscillator harmonics fall within the received band. Other harmonic rejection techniques come in handy in situations where wideband operation is required. An example of such techniques is harmonic reject mixers.

1.2.4.1 Harmonic Reject Mixers

The proposed receiver operates at 30~510 MHz. For signals lying at (30~170 MHz), local oscillator harmonics up to the 17th harmonic fall within the receiver's band. The principle of harmonic reject mixers depends on the idea that unwanted harmonics result from mixing unwanted signals at LO harmonics with the LO harmonics, thus, in order to reject such signals we could reduce LO harmonics of mixers instead of reducing the power of the signal to be mixed using filters. Basically, the switching mixer output can be regarded as the RF signal multiplied by the square wave version of the LO. A 50% duty cycle square wave can be expressed in the form

$$P_o(t) = \frac{4}{\pi}[A_{LO}(cos(w_{LO}t) - \frac{1}{3}cos(3w_{LO}t) - \frac{1}{5}cos(5w_{LO}t) - \frac{1}{7}cos(7w_{LO}t)...]$$

The 3^{rd} and 5^{th} harmonics in the above equation can be cancelled by applying a 2 step technique. First, we generate a square wave with opposite sign in the harmonics-to-be-rejected coefficients. Then, we add these square waves together with proper amplitude scaling to remove the harmonics part. A 45 degree phase shift is the simplest way to cancel the 3^{rd} and 5^{th} harmonics where two extra square waves with the fundamental phase shift of $\pm\frac{\pi}{4}$ are required.

The 3rd and 5th Harmonic rejection can be proved as follows:

$$P_o(t) = \frac{4}{\pi}\left(cos(\omega t) - \frac{1}{3}cos(3\omega t) + \frac{1}{5}cos(5\omega t)\ldots\right)$$

$$P_{1,2}(t) = \frac{4}{\pi}\left(cos\left(\omega t \pm \frac{\pi}{4}\right) - \frac{1}{3}cos\left(3\omega t \pm \frac{3\pi}{4}\right) + \frac{1}{5}cos\left(5\omega t \pm \frac{5\pi}{4}\right)\ldots\right)$$

$$\begin{aligned} P_{1,2}(t) = \frac{4}{\pi}\Big(&\left[cos(\omega t)\cos\left(\pm\frac{\pi}{4}\right) - \sin(\omega t)\sin\left(\pm\frac{\pi}{4}\right)\right] \\ &- \frac{1}{3}\left[cos(3\omega t)\cos\left(\pm\frac{3\pi}{4}\right) - \sin(3\omega t)\sin\left(\pm\frac{3\pi}{4}\right)\right] \\ &+ \frac{1}{5}\left[cos(5\omega t)\cos\left(\pm\frac{5\pi}{4}\right) - \sin(5\omega t)\sin\left(\pm\frac{5\pi}{4}\right)\right]\ldots\Big) \end{aligned}$$

$$\begin{aligned} P_{1,2}(t) = \frac{4}{\pi}\Big(&\left[cos(\omega t)\cos\left(\frac{\pi}{4}\right) \mp \sin(\omega t)\sin\left(\frac{\pi}{4}\right)\right] - \frac{1}{3}\left[cos(3\omega t)\cos\left(\frac{3\pi}{4}\right) \mp \sin(3\omega t)\sin\left(\frac{3\pi}{4}\right)\right] \\ &+ \frac{1}{5}\left[cos(5\omega t)\cos\left(\frac{5\pi}{4}\right) \mp \sin(5\omega t)\sin\left(\frac{5\pi}{4}\right)\right]\ldots\Big) \end{aligned}$$

$$P_1(t) + P_2(t) = \frac{8}{\pi}\left(\left[cos(\omega t)\cos\left(\frac{\pi}{4}\right)\right] - \frac{1}{3}\left[cos(3\omega t)\cos\left(\frac{3\pi}{4}\right)\right] + \frac{1}{5}\left[cos(5\omega t)\cos\left(\frac{5\pi}{4}\right)\right]\ldots\right)$$

$$P_1(t) + P_2(t) = \frac{4\sqrt{2}}{\pi}\left(cos(\omega t) + \frac{1}{3}cos(3\omega t) - \frac{1}{5}cos(5\omega t)\ldots\right)$$

$$P_o(t) * \sqrt{2} + P_1(t) + P_2(t) = \frac{4\sqrt{2}}{\pi}\left(3\,cos(\omega t) + 7^{th}\ and\ higher\ harmonic\ components\right)$$

It can be shown that in order to eliminate up to 9^{th} harmonic we would need 4 extra square waves and to remove up to the 13^{th} harmonic we would need 6 extra square waves. But for all practical purposes elimination of the 3^{rd} and 5^{th} harmonics is enough as adding 2 extra square waves means having 3 mixers instead of one, or rather 6 instead of 2. To eliminate the 7^{th} and 9^{th} it would take 10 mixers instead of 2 hence introducing a rather non affordable complexity. For ideal harmonic reject mixers, the harmonic rejection ratio (HRR) is infinite. However, harmonic rejection ratio is practically finite due to amplitude mismatch and phase imbalance. Sophisticated calibration schemes are carried out if high HRR is required.

1.2.5 Image Rejection Techniques

Image is one of the most infamous problems facing the implementation of heterodyne radios. Image rejection is desirable yet the amount of rejection varies from one standard to another. While some standards require Image Rejection Ratio (IRR) in the range of 30 dB (like GSM), other standards impose a high IRR (more than 60 dB). Image Rejection gets tricky when using low IF because the signal and the Image are at 2 FIF frequency separation; hence making it impossible to use the conventional image reject SAW filter. The following are image rejection techniques that are used when the system has a low IF.

1.2.5.1 Hartley and Weaver Architectures

The Hartley Structure and the Weaver Structure are the most famous methods for implementing Image Rejection. They have been introduced decades ago yet, the achievable image rejection ratio (IRR) for such architectures has been limited to 30 to 35 dB because these structures are highly sensitive to mismatches. Both architectures rely on the idea of creating two signals, where the Image in both signal is of different polarity while the polarity of the desired signal is the same. Then by adding these 2 signals the image cancels out and the required signal remains.

The two signals being generated are basically generated by means of a 90 degree phase shift between both signal paths. In time domain, a 90 degree phase shift converts sin(wt) to cos(wt) and converts cos(wt) to -sin(wt). While in frequency domain, this is equivalent to multiplying the signal by G(w)=-j.sign(w), which basically is multiplying the right half plane of w by -j and which basically is multiplying the left half plane of w by +j.

The Hartley architecture generates the 90 degree phase shift in the path by means of an RC-CR Network. Figure 7 shows an example of a Hartley mixer. The Low-Pass/High-Pass effect provides a constant phase shift of 90 degrees at all frequencies yet, it provides matched gain only at the 3-dB BW (w=1/RC) given that there are no mismatch between R and C and the I and Q paths are perfectly balanced. If we take into consideration the mismatch in gain and phase in both signal paths due to the component tolerance of the resistance and the capacitance, along with the mismatch between the quadrature components of the LO the image rejection of the Hartley architecture gets highly deteriorated.

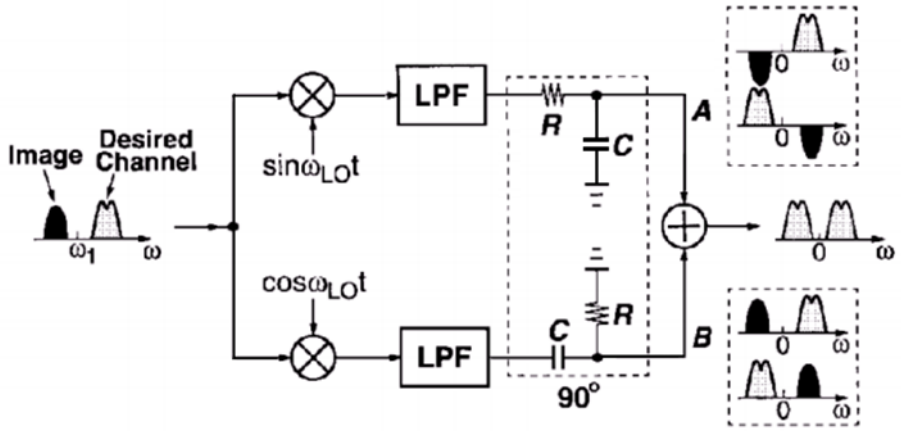

Figure 7: Hartley Image Reject Receiver

The Weaver architecture on the other hand implements the 90 degrees phase shift by means of a second mixing stage. Figure 8(a) shows a basic weaver mixer structure and figure 8(b) shows the graphical analysis for the Weaver architecture. While the Weaver is not susceptible to the problems that arise from the mismatch in gain due to the RC-CR like in the Hartley structure, it suffers from a rather more severe problem, which is the secondary image for the second set of mixers. If the second set of mixers do not translate the signal to DC then as shown in figure 5 a second image at the first IF will down-convert with the desired signal to the second IF deteriorating IRR. Also, the Weaver architecture suffers from the mismatches in phase and amplitude for the LO quadrature signals.

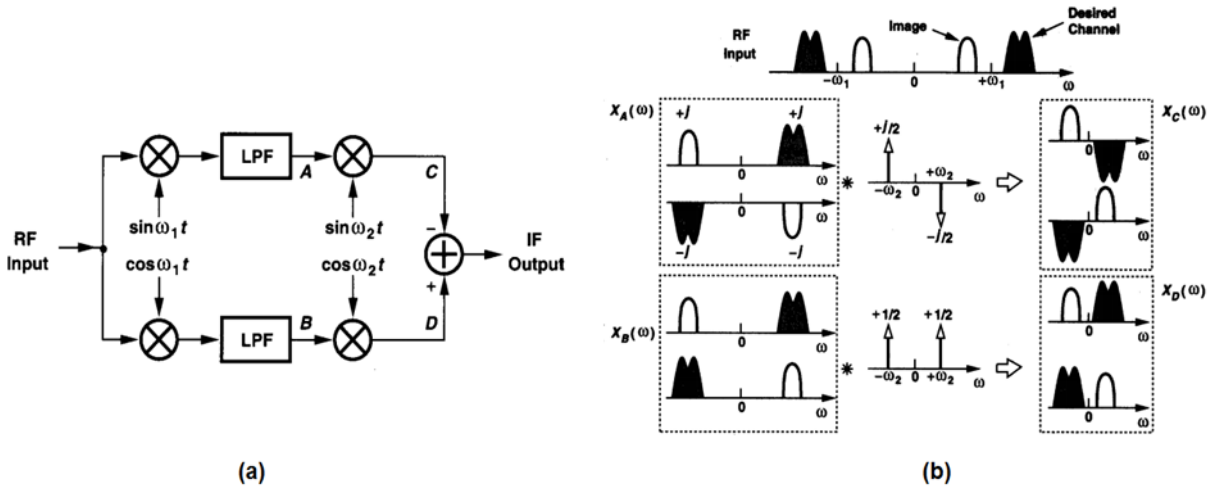

Figure 8: (a) Weaver Structure and (b) Graphical Analysis of The Weaver structure

1.2.5.2 Quadrature Mixing and Complex Filters

Another methodology to better image rejection is quadrature mixing alongside using complex filters (Poly-phase Filters (PPF)). The idea of such structures lies mainly in mixing the signal with only one side of the sinusoid (a natural exponential). The natural exponential translates the signal to one side of the spectrum while translating the image to the other. Then, using a complex filter -that has a different response on one side of the spectrum than the other- the image gets filtered away. The single quadrature mixing is the most basic form for such structures. As Shown in figure 9(a) the RF input is mixed with two quadrature LO signals

and the quadrature outputs of the mixer are processed by the image reject poly-phase filters. The RF input can be expressed as $A_{RF}cos(w_{RF}t)$ *and* $A_{IM}sin(w_{IM}t)$; the ideal quadrature LO signals can be expressed as $A_{LO}cos(w_{LO}t)$ *and* $A_{LO}sin(w_{LO}t)$ where A_{RF}, A_{IM}, and A_{LO} are the amplitudes of the RF signal, the image signal, and the local oscillator respectively. Assuming no amplitude or phase mismatch between the LO quadrature signals, the quadrature LOs can be combined and viewed as a complex LO signal $A_{LO}e^{jw_{LO}t}$ and the quadrature output of the mixer can be expressed as:

$$[A_{RF}cos(w_{RF}t) \; and \; A_{IM}sin(w_{IM}t)] \, A_{LO}e^{jw_{LO}t}$$

Assuming high side injection where $w_{LO} - w_{RF} = w_{IM} - w_{LO} = w_{IF}$ the output can be simplified to $\frac{1}{2}A_{RF}A_{LO}e^{jw_{IF}t} + \frac{1}{2}A_{IM}A_{LO}e^{-jw_{IF}t}$ separating the RF signal and the Image as positive and negative frequency components respectively. The poly-phase filter lets the desired signal and attenuates the negative frequency image signal. Image rejection would then be determined by how hard the complex filter would attenuate the image at the negative frequency.

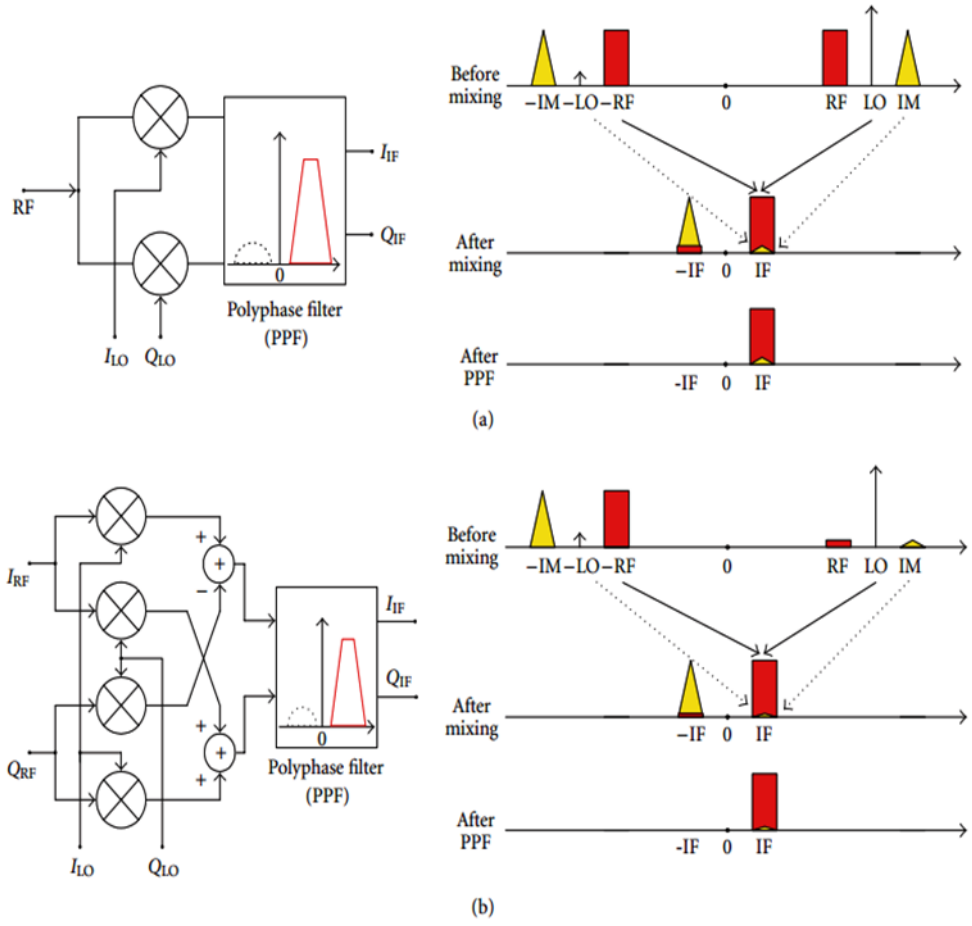

Figure 9: (a) Single Quadrature Structure and (b) Double Quadrature Structure

Practical device mismatch greatly reduces IRR of such a structure. Gain and phase mismatch for the LO signals and mismatch between the 2 mixers would result in a portion of the sinusoid appearing at the part of the natural exponential that was deemed to vanish. IRR due to device mismatch could be calculated as:

$$IRR \approx \frac{1}{4}\left[\left(\frac{\Delta A}{A}\right)^2 + (\tan(\Delta\Phi))^2\right],$$

where ΔA is the overall gain mismatch between I/Q paths and A is the nominal gain,$\Delta\Phi$ is the overall phase imbalance in radians. Both ΔA and $\Delta\Phi$ are determined by the LO and mixer's mismatch as shown below:

$$\frac{\Delta A}{A} \approx \frac{\Delta A_{LO}}{A_{LO}} + \frac{\Delta G_{Mixer}}{G_{Mixer}}, \qquad \tan(\Delta\Phi) \approx \tan(\Delta\Phi_{\mathrm{LO}}) + \tan(\Delta\Phi_{\mathrm{Mixer}})$$

To achieve 60 dB IRR, both LO phase imbalance and and mixer normalized gain mismatch should be less than 0.1 degrees and 0.1% respectively. Mixer gain mismatch could be overcome by means of passive mixing and good layout yet, LO phase imbalance usually supersedes 1 degree even with proper calibration implying no more than 40 dB IRR.

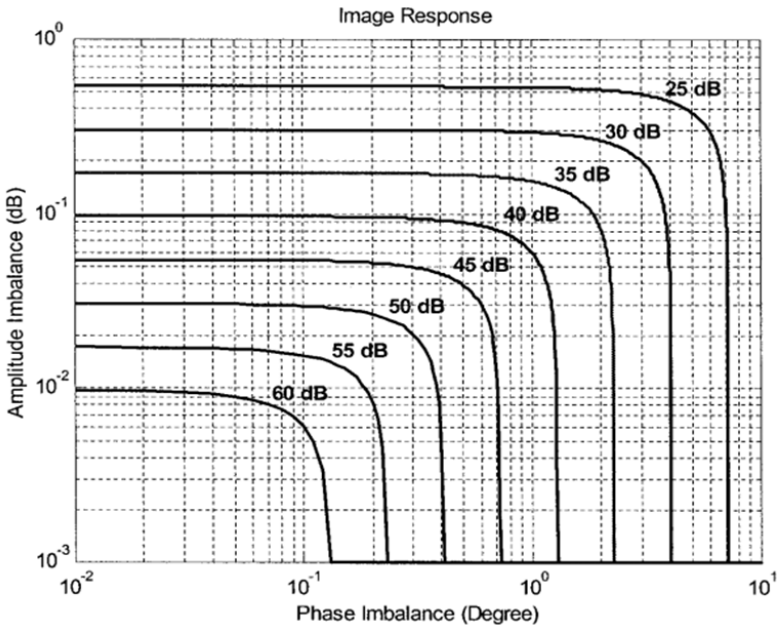

Figure 10: Image Rejection Ratio vs. Amplitude mismatch and Phase Imbalance

The double quadrature mixing relaxes the condition on amplitude mismatch and phase imbalance of the LO. As shown in Figure 9(b) the RF is first split into I/Q paths then the mixing is carried out between I/Q of the RF and I/Q of the LO. This results in doubling the number of mixers and added system complexity. The IF signal can be expressed as follows:

$$I_{IF} + j\,Q_{IF} = (I_{RF} + j\,Q_{RF}) \times (I_{LO} + j\,Q_{LO}) = (I_{RF}I_{LO} - Q_{RF}Q_{LO}) + j(I_{LO}Q_{RF} + Q_{LO}I_{RF}).$$

Because the RF input is complex, only the negative frequency components (desired RF and undesired image signals) are present at the input of the mixer. Considering the mismatch between the I/Q paths, part of the positive frequency will be pass through to the mixer input. The undesired positive image and negative LO will result in Image power being translated to IF but with higher rejection than single quadrature mixing. The overall gain mismatch and phase imbalance for double quadrature architecture are obtained as:

$$\frac{\Delta A}{A} \approx \frac{\Delta A_{LO}}{A_{LO}}\frac{\Delta A_{RF}}{A_{RF}} + \frac{\Delta G_{Mixer}}{G_{Mixer}}, \qquad \tan(\Delta\Phi) \approx \tan(\Delta\Phi_{\mathrm{RF}}) \times \tan(\Delta\Phi_{\mathrm{LO}}) + \tan(\Delta\Phi_{\mathrm{Mixer}})$$

Hence, to achieve 60 dB IRR, assuming 0.1% mixer gain mismatch, only 2.4 degree phase imbalance and 3% gain mismatch are required for the quadrature RF and LO, which can be achieved even without sophisticated calibration.

1.2.5.3 Digital Dual Quadrature Down-Converter

A rather effective digital solution for increasing receiver's IRR is the Digital Dual Quadrature down-converter. The digital dual quadrature receives the RF I and Q components and calibrates for the I/Q mismatch digitally. Then, it uses the same technique as in double quadrature down conversion mentioned above using digital mixers and digital LOs. Digital mixers do not suffer the problems their analog counterparts do, there is no phase imbalance and there is nearly zero gain mismatch. Figure 11 shows a typical Digital Dual Quadrature down-conversion scheme. Such systems produce as high IRR as 60~70 dB on the cost of extra digital hardware.

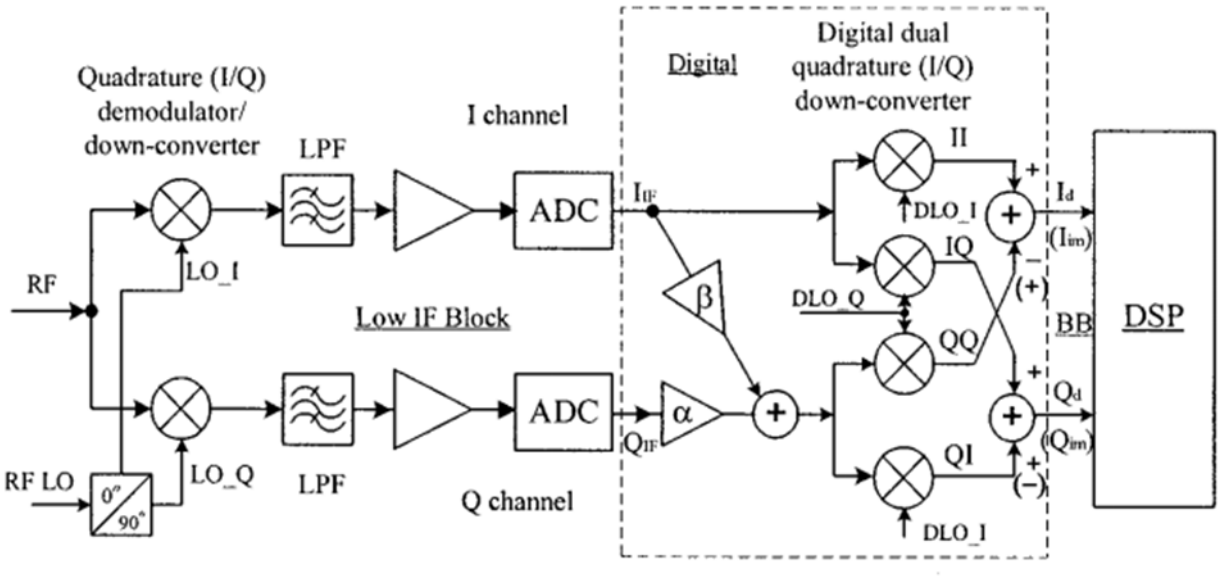

Figure 11: Digital Dual Quadrature Down-Conversion Structure

1.3 Sub-sampling Receiver

Sub-sampling Receivers do benefit from the infamous property of aliasing in ADCs. A typical ADC samples the continuous analog domain to the discrete domain where the bandwidth depends on the ADC sampling frequency (Fs) and is equal to Fs/2. Signals lying at frequencies higher than Fs/2 get aliased from both the positive and negative frequency domain into the Fs/2 zone. The ADC acts as a mixer mixing down signals by harmonics at sampling frequency and its harmonics. In order to ensure a non-destructive aliasing, the sampling frequency should be greater than twice the channel bandwidth. Sub-sampling is a viable solution for broadband receivers for it deploys a relaxed ADC bandwidth and the ability to process high IF signals with a reasonable sampling frequency. The sampling rate in sub-sampling receivers depends on the information signal bandwidth instead of the highest frequency hence reducing the processing rate.

2 PROPOSED RECEIVER

The proposed architecture is driven by the nature of the required system. To achieve the best of a frequency hopping system, settling time of tunable blocks of the system has to be considered. The system is expected to cover a frequency range of 30-510 MHz and the main standard's channel bandwidth is 5, 10, or 25 kHz with 25 kHz channel spacing. Such narrow channel spacing with such wide system bandwidth would force a very high settling time for the Phase Locked Loop (PLL). Hence, the job of selecting the channel is divided between the PLL, the IF

Filter, and the ADC. The bandwidth is divided into 8 divisions each comprising a 60 MHz to be down-converted to IF band of 30-90 MHz. The IF is then filtered via A Hopping Complex band-pass filter, amplified via Automatic Gain Control, then fed to a sub-sampling ADC operating at 20 MSPS. The sampling rate of the ADC is chosen so the IF is divided to 3 sub-divisions each 20 MHz wide. The Hopping filter is to select a band where the required image lies and to filter out noise and image imposed by ADC aliasing. The AGC is deployed to achieve a proper signal level for the ADC to have a proper SQNR. Channel selection and filtering is to be carried out in digital domain via DSP. Harmonic rejection is carried out via harmonic reject mixers to suppress only 3rd and 5th harmonics. Harmonic Rejection is only applied to the divisions lying at 90-150 MHz and 150-210 MHz. The 30-90 MHz division bypasses the mixers and the divisions lying at frequencies greater than 210 MHz have no odd harmonics in band. Image rejection is to be carried out via Double Quadrature Mixing and Complex Filtering. The target Image rejection ratio is more than 60 dB. Figure 12 shows the proposed receiver block diagram.

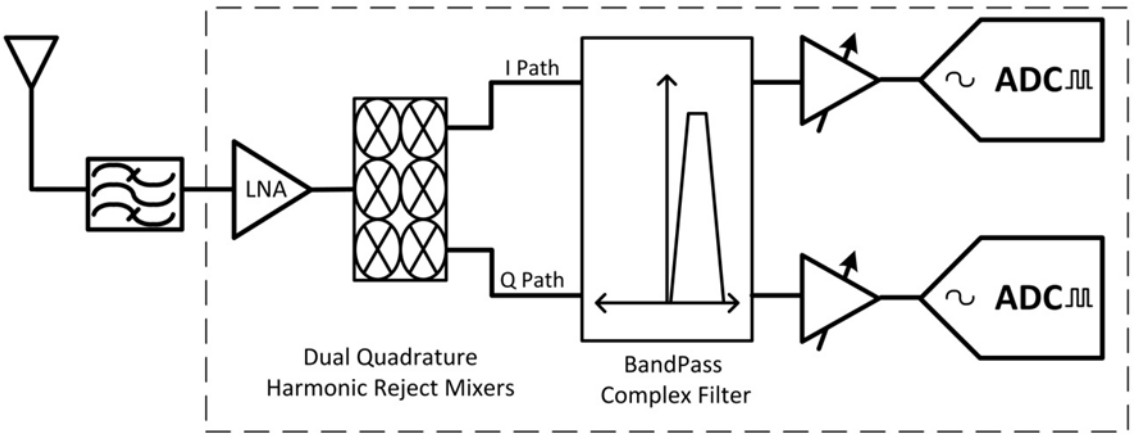

Figure 12: Proposed Receiver Block Diagram

2.1 System Budget

2.1.1 Required Top Level System Specifications

The top level system specifications are normally extracted from specific standards. The target design is a front end that is compatible with the first Manpack Transceiver version and configurable for future Multi-Standard versions. The first Manpack Transceiver version targeted the Single Channel Ground and Airborne Radio system (SINCGARS).

Noise Figure

Sensitivity is defined as the minimum detectable signal level a receiver can detect to provide a required signal to noise ratio (SNR) at the end of the receiver chain. The required SNR for SINCGARS is typically 10 dB and the sensitivity is -120 dBm. Assuming matched impedance between the LNA and the band-select filter the overall system noise figure can be calculated as:

$$NF = S_{in} - 10\log(kT) - 10\log(BW) - SNR$$

Where Sin is the system's sensitivity, k is Boltzman's constant, BW is the channel bandwidth, and SNR is the required SNR at the end of the receiver. For a sensitivity of -120 dBm, BW of 5 KHz, and SNR of 10 dB the system's noise figure is calculated to be 7 dB.

Linearity

The IIP3 of a receiver is set so as to make the third-order intermodulation product lower than the maximum interference level which in turns is equal to the noise power concealed within the channel.

$$P_{IM3} = 10\ \log(kT\ \times BW) + NF$$

Hence the calculated IM3 level is -130 dBm. Therefore, to sustain proper operation under interferers 70 dB higher than sensitivity level the system's IIP3 is calculated as

$$IIP3 = (3\ P_{in} - \ P_{IM3})/2$$

where Pin is the two-tone input interference level in decibel mW. For Interferers as large as -50 dBm the system's IIP3 is calculated to be -10 dBm.

2.1.2 System Gain Distributions

The system transmits power at 1 Watts up to 50 watts. Assuming a minimum distance of 500 meters with 1 W transmitted power, according to Friis transmission equation path loss is calculated as:

$$L = C\ \log\left(\frac{4\ \pi\ d}{\lambda}\right)$$

where C is a constant that is roughly equal to 35 in case of VHF/UHF signals propagating over the surface of the earth. For a 100 meters distance the path loss is 74 dB and 116 dB for 30 MHz and 510 MHz signals respectively.

For 30 dBm transmitted signal the maximum received signal for a 100 meters distance is -44 dBm. The system will account for a gain control scheme for a received signal of -120 to -40 dBm. The ADC is to have a full scale signal of 1.5 Vpp corresponding to 7.5 dBm. Accounting for PAPR of 7.5 dB the signal ought to be at the level of 0 dBm at the input of the ADC. Table 1 demonstrates the system gain distribution and signal levels.

Table 2: System Gain Distribution and Signal Levels

	Gain (dB)	Input Level (dBm)	Output level (dBm)
LNA	20	-120 ~ -40	-100 ~ -20
Mixer	10	-100 ~ -20	-90 ~ -10
Band-pass Filter	10	-90 ~ -10	-80 ~ 0
Variable Gain Amplifier	0 ~ 40	-80 ~ 0	-40~0

2.1.3 System Noise Figure

Noise figure is defined as the ratio between input and output SNR in dB. A system's noise figure is calculated as:

$$F = \frac{SNR_i}{SNR_o} = \left(\frac{S_i}{k\ TB}\right)\Big/\left(\frac{S_o}{N_o}\right) = \left(\frac{S_i}{k\ TB}\right)\left(\frac{N_o}{S_o}\right) = \frac{1}{G_{AV}}\left(\frac{N_o}{kTB}\right), \qquad NF = 10\log(F)$$

Where N_o is the available noise power at the output of the system and GAV is the available power gain of the system. Si and So are the available input and output signal power respectively. For cascaded systems, Friis has proved the noise figure of the network as:

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_{AV,1}} + \frac{F_3 - 1}{G_{AV,1}G_{AV,2}} + \cdots \frac{F_n - 1}{G_{AV,1}G_{AV,1} \ldots G_{AV,n-1}}$$

Where Fi is the noise figure of the stage i with respect to a source impedance of ROUT,i-1and GAV,i is the available power gain of stage i. Friis' approach served the discrete RF receiver designs well when the input and output impedance of most building blocks in the receiver were matched to a standard value usually 50Ω. In integrated receivers, the impedance of individual blocks is usually unknown and different and applying the Friis formula without knowing these values would be erroneous. Hence NF is calculated using loaded voltage gain and input referred noise.

The output noise of a system can be referred to input as a noise voltage source:

$$\overline{v_{n,i}^2} = \overline{v_{n,o}^2}/A_{vn}^2$$

where A_{vn}^2 is the loaded voltage gain, the loaded voltage gain is the voltage gain of a stage taking into account the loading effect of the next stage $A_{vn} = A_v(\frac{R_L}{R_L+R_{OUT}})$. It can be proved that the cascaded loaded voltage gain is the product of all the cascaded stages' loaded voltage gains. The cascaded NF can be calculated from the total noise voltage referred the input of the system.

For a fully integrated receiver the total input referred noise at the first stage is equal to:

$$\overline{v_{ni,tot}^2} = \overline{v_{ni,1}^2} + \frac{\overline{v_{ni,2}^2}}{A_{vn,1}^2} + \frac{\overline{v_{ni,3}^2}}{A_{vn,1}^2 A_{vn,2}^2} + \ \ldots$$

Assuming a 50Ω discrete RF filter (or antenna switch) output impedance and First stage input impedance of Rs, noise figure can be calculated as:

$$F = \frac{4kT\times 50 + \overline{v_{ni,tot}^2}\left(\frac{R_s+50}{R_s}\right)^2}{4kT\times 50} = 1 + \frac{\overline{v_{ni,tot}^2}\left(\frac{R_s+50}{R_s}\right)^2}{4kT\times 50}$$

For $R_s = 50\Omega$ Noise figure is expressed as:

$$F = 1 + \frac{\overline{v_{ni,tot}^2}}{kT\times 50} = 1 + \frac{\overline{v_{ni,1}^2}}{kT\times 50} + \frac{\overline{v_{ni,2}^2}}{A_{vn,1}^2 \times kT\times 50} + \frac{\overline{v_{ni,1}^2}}{A_{vn,1}^2 A_{vn,2}^2 \times kT\times 50} + \ \ldots$$

This is analogous to Friis expression, except that Noise Figure for each block is calculated as:

$$F_i = 1 + \frac{\overline{v_{ni,i}^2}\left(\frac{R_s + R_1}{R_s}\right)^2}{4kT \times 50}$$

Where $\overline{v_{ni,i}^2}$ is the input referred noise of system i, measured in V^2/Hz, R_s is the input impedance of the first block in the chain, and R_1 is the output impedance of the block feeding the first block in the receiver chain. The overall noise figure can then be calculated as:

$$F_{tot} = F_1 + \frac{F_2 - 1}{A_{vn,1}^2} + \frac{F_3 - 1}{A_{vn,1}^2 A_{vn,2}^2} + \cdots \frac{F_n - 1}{A_{vn,1}^2 A_{vn,2}^2 \cdots A_{vn,n-1}^2}$$

Hence, block level noise figure is calculated as:

$$F_{tot} = F_{LNA} + \frac{F_{Mixer} - 1}{100} + \frac{F_{Filter} - 1}{1000} + \frac{F_{VGA} - 1}{10^4} + \frac{F_{ADC} - 1}{10^8}$$

To achieve the required 7 dB noise figure F_{tot} must not exceed 5.011. The main contributors to the noise figure are the LNA, the Mixer, and the first filter for filters exhibit a relatively high input referred noise. The RF Switch is assumed to have an attenuation of 2 dB which decreases the required system noise figure from 7 dB to 5 dB (Ftot not exceeding 3.162).

Typical well-designed wideband LNAs exhibit a Noise Figure of 1 dB (F = 1.26). The mixers should have input referred noise level of 5 nV/√Hz corresponding to F = 123.6 hence contributing an additional 1.226 to F_{tot}.

The First Filter should have 10 nV/√Hz noise level corresponding to F = 494.4 hence contributing 0.493 to Ftot. The first VGA noise level is at 5 nV/√Hz contributing 0.012 to F_{tot}. The Analog to Digital Converter (ADC) should have noise level of 1.85 uV/√Hz to fulfill the required noise figure. That corresponds to Total SNR of 49 dB requiring effective number of bits (ENOB) of 8 bits. Table 2 shows block level noise figure and required input referred noise.

Table 3: Block Level Noise Figure and Input-referred Noise

	Gain (dB)	NF (dB)	Input referred Noise (nV/√Hz)	Total NF at Block Output
LNA	20	1	0.5	1
Mixer	10	21	5	3.95
Band-pass Filter	10	27	10	4.74
Variable Gain Amplifier	0 ~ 40	21	5	4.76
ADC	0	72	1850	5

2.1.4 System Linearity

The Input Intersect Point 3 (IIP3) is a very important linearity measure for a radio receiver. The required receiver IIP3 was calculated in section 2.2.1 to be -10 dBm. For a cascade of systems, and assuming all 3^{rd} intermodulation product terms are in phase, the total IIP3 is calculated as:

$$\frac{1}{V_{iip3,tot}^2} = \frac{1}{V_{iip3,1}^2} + \frac{A_{vn,1}^2}{V_{iip3,2}^2} + \frac{A_{vn,1}^2 A_{vn,2}^2}{V_{iip3,3}^2} + \cdots + \frac{A_{vn,1}^2 A_{vn,2}^2 \cdots A_{vn,n-1}^2}{V_{iip3,n}^2}$$

When a block is preceded by a filter, the attenuation to the 2-tone interferer by X dB is equivalent to increasing a block's IIP3 by 1.5*X dB. Assuming the band-pass filter would highly attenuate the 2-tone interferer, IIP3 will be mainly affected by the LNA and the mixer, and the total IIP3 will be reduced to:

$$\frac{1}{V_{iip3,tot}^2} = \frac{1}{V_{iip3,LNA}^2} + \frac{100}{V_{iip3,mixer}^2}$$

$$100 = \frac{1}{V_{iip3,LNA}^2} + \frac{100}{V_{iip3,mixer}^2}$$

Hence, $v^2_{iip3,LNA}$ is required to be $0.1\,V^2$ and $v^2_{iip3,MIXER}$ is required to be $1.11\,V^2$. Hence LNA IIP3 is equal to 0 dBm ($0.316\,V_{PK}$) and Mixer IIP3 is equal to 10.45 dBm ($1.05\,V_{PK}$).

2.2 Block Level Specifications

2.2.1 Wideband LNA

The main challenges facing LNA design are the very low noise requirement and the wide band of operation. Table 3 shows the LNA specifications

Table 4: LNA Specifications

Low Noise Amplifier				
Parameters	Min.	Typ.	Max.	Units
Gain		20		dB
Input Referred Noise			0.5	nV/√Hz
Input Impedance		50		Ω
Low 1 dB Frequency		30		MHz
High 1 dB Frequency		510		MHz
Input 1 dB Compression Point	0.11			V_{PK}
IIP3	0			dBm

2.2.2 Harmonic-Rejection Quadrature Mixers

Mixing entails 2 techniques in the proposed architecture: Double Quadrature for Image Rejection and Multi-Phase Mixing for Harmonic Rejection. For Double Quadrature scheme 4 Mixing sets are required, and For Multi-Phase Scheme each set would have 3 Mixers. The 3 Mixers are divided to one Primary Mixer having a gain equal to 0.45 dB and two secondary mixers having a gain equal to -5.54 dB For the combination to provide 10 dB of gain. Table 4 shows the mixer specifications.

Table 5: Mixers Specifications

Mixers					
Parameters	Min.	Typ.	Max.	Step	Units
Primary Voltage conversion Gain		0.45			dB
Secondary Voltage Conversion Gain		-2.54			dB
Input Referred Noise			5		nV/√Hz
RF input Frequency Range	30		510		MHz
LO Input Frequency Range	60		420	60	MHz
RF Input 1 dB Compression Point	0.35				V_{PK}
RF IIP3	10.45				dBm

2.2.3 Complex Hippong Bandpass Filter

The Complex Band-pass Filter wil play a major rule in image rejection. The Filter Hops between different sub-divisions to (1) attenuate the white noise that would deteriorate the sub-samplig ADC performance and (2) Reject the Adjacent Interferers to allow for relaxed linearity constraints on the VGA.

Table 6: Complex Filter Specifications

Baseband Complex Filter					
Parameters	Min.	Typ.	Max.	Step	Units
Center Frequency	32		88	4	MHz
-1 dB bandwidth		4			MHz
Input Referred Noise			10		nV/√Hz
Pass-band Gain		10			dB
Attenuation at 2.5 F_C	24				dB
Maximum Pass-band Ripple			1		dB

2.2.4 Automatic Gain Control

Automatic Gain Control is realized via a Variable Gain Amplifier and a received signal strength indicator (RSSI). The AGC control is digital via DSP and the RSSI senses the power at the VGA output and feeds back the back-end to generate the digital word for VGA Gain Control.

Table 7: Variable Gain Amplifier Specifications

Variable Gain Amplifier					
Parameters	Min.	Typ.	Max.	Step	Units
Gain	0		40	5	dB
Input Referred Noise			5		nV/√Hz
Low 1 dB Frequency		30			MHz
High 1 dB Frequency		90			MHz
IIP3	10				dBm

2.2.5 Subsampling Analog to Digital Converter

The Analog to Digital Converter is to have a 20 MHz sampling rate. The total input referred noise of the ADC is expected to fall at $1.85\mu V/\sqrt{Hz}$ requiring ENOB equal to 8. Table 7 shows the required ADC specifications.

Table 8: ADC Specifications

Analog to Digital Converter				
Parameters	Min.	Typ.	Max.	Units
Total SNIR	50			dB
DNL & INL			0.5	LSB
Full Scale Swing	1.5			$V_{PP,diff}$

3 TRANSMITTER ARCHITECTURES

Most transmitter topologies are analogous to receiver topologies discussed in the previous sections. A Digital to Analog Converter (DAC) converts the signal from the digital domain to the Analog domain, the DAC generates replicas of the signal in the analog domain at sampling rate harmonics and a filter is used to hold onto just one of these replicas. The signal is then translated to the frequency of interest by means of mixing stage(s) and then a Power Amplifier (PA) is used to elevate the signal's power to the required level. A transmitter's sole purpose is to provide maximum power to the output signal while filtering the out-of-band components that result from the PA nonlinearity. Since the signal is generated via the DAC hence having

a proper amount of power, noise is no major concern in transmitters like they are for the receivers. Linearity, on the other hand, is problematic for signal amplitudes in Tx path are large by nature.

3.1 Direct Conversion Transmitter

A direct conversion Transmitter depends on a single translation step in frequency. A quadrature up-conversion mixer is used to up-convert the baseband signal to the required RF frequency. Figure 13 shows a typical direct conversion transmitter.

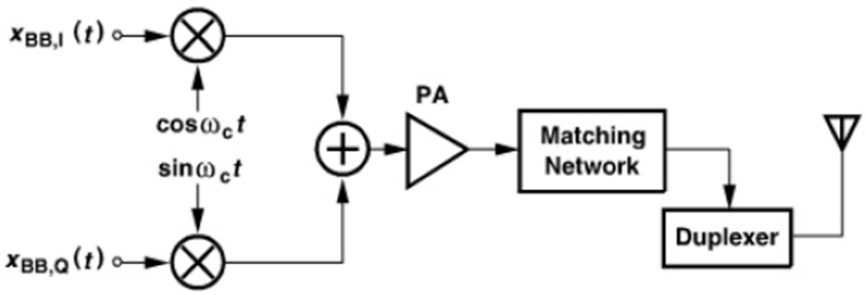

Figure 13: Direct Conversion Transmitter

Direct conversion suffers from some major problems such as:

1. Carrier Leakage: Carrier leakage can result from a DC offset in the DAC propagating to the mixer and causing a single tone in the middle of the transmitted signal.

2. Oscillator pulling: The PA output exhibits a very large swing which couple to various parts of the system through substrate leakage. The PA's coupled output may interact with the Local Oscillator causing the VCO to deviate from its required center frequency.

And due to the fact that the local oscillator is a very delicate and area consuming block, transmitters are almost always analogous to receivers in frequency planning. So, a heterodyne approach is being admitted for the Tx.

3.2 Proposed System

The up-conversion process is to be carried out in two steps. First, the signal is translated to the frequency of interest by means of a digital mixer. The Signal is then fed to a 200 MSPS DAC that covers the whole IF range (30~90 MHz). Then, a band-pass filter omits the out of band noise and the signal is applied to a linear, efficient power amplifier for amplification. The power amplifier is the most power-hungry component on-chip. Higher efficiency results in less power consumption and less heat dissipation issues. Figure 14 shows the proposed transmitter architecture.

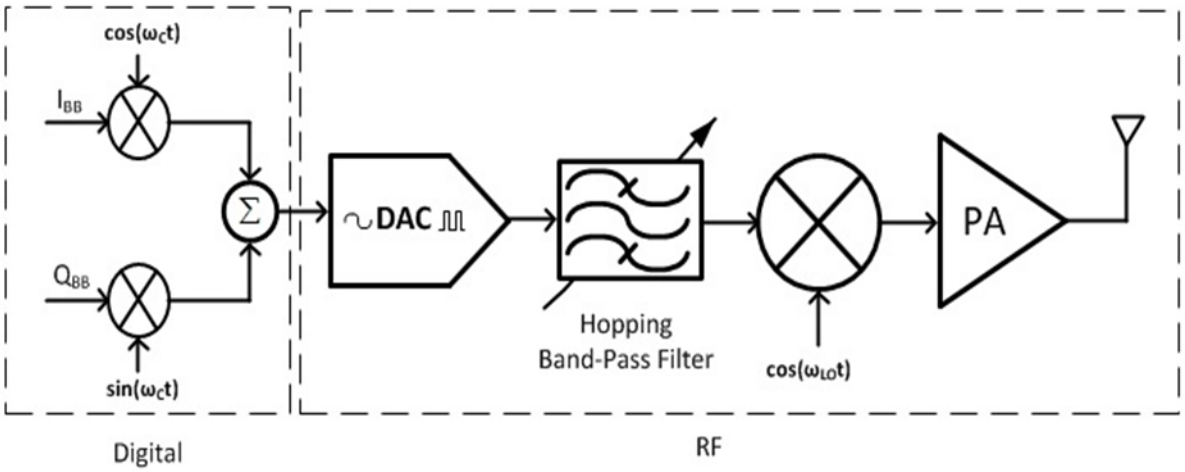

Figure 14: Proposed Transmitter Block Diagram

3.3 Block Level Specifications

3.3.1 Digital to Analog Converter

Table 9: Digital to analog Converter Specifications

Digital To Analog converter				
Parameters	Min.	Typ.	Max.	Units
Resolution		12		Bit
Integral Non Linearity			2	LSB
Full Scale Swing	1			$V_{PP,diff}$
Sampling Rate	200			MSPS
Settling Time	100			pS

3.3.2 Bandpass Hopping Filter

The band-pass filter filters out the out of band noise to meet the power spectral emission specifications. Table 9 shows the band-Pass filter specifications.

Table 10: Band-Pass Filter Specifications

Band-Pass Filter					
Parameters	Min.	Typ.	Max.	Step	Units
Center Frequency	32		88	4	MHz
-1 dB bandwidth		4			MHz
Pass-band Gain		0			dB
Attenuation at 2.5 F_C	24				dB
Maximum Pass-band Ripple			1		dB

3.3.3 Up Conversion Mixer

The up-conversion mixer has no constraint regarding noise. Linearity on the other hand is a very important aspect while designing mixers. Table 10 shows the up-conversion mixer specifications.

Table 11: Up-Conversion Mixer Specifications

Up-conversion Mixer					
Parameters	Min.	Typ.	Max.	Step	Units
Primary Voltage conversion Gain		10			dB
RF output Frequency Range	30		510		MHz
LO Input Frequency Range	60		420	60	MHz
RF Output 1 dB Compression Point	0.5				V_{PK}

3.3.4 Envelope Tracking Power Amplifier

A Class AB envelope tracking power amplifier is proposed. The AB operation provides high linearity and a broad bandwidth and envelope tracking provides high efficiency at back-off operation. Table 11 shows the power amplifier specifications.

Table 12: Power Amplifier Specifications

Power Amplifier				
Parameters	Min.	Typ.	Max.	Units
Output Power		30		dBm
-1 dB bandwidth		510		MHz
Gain		15		dB
PAE	60			%
EVM (QPSK)			4	%

Part II
Digital-to-Analog Converter

4 INTRODUCTION

Many architectures of DACs are found in literature. Also these architectures are implemented in different ways. Some of these architectures are Binary-weighted DACs, Thermometer-coded DACs, Algorithmic DACs, and finally Hybrid DACs where different architectures are combined to form make use of their advantages together. One popular hybrid architecture is the so called segmented architecture where the most significant bits is encoded into thermometer code and the least significant bits are binary weighted. On the other hand, these architectures could be implemented using different ways, such as Current-Steering DACs, Charge-Redistribution DACs, and Resistor-Ladder DACs. Among all these various architectures and implementation ways, Segmented Current-Steering DACs are the favorite ones for many designers, especially when the application demands a high-speed high-resolution DAC. These make use of the speed – that nowadays can reach up to 2.9 GHz – of Current-Steering implementation and the great performance concerning Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) of the Segmented architecture.

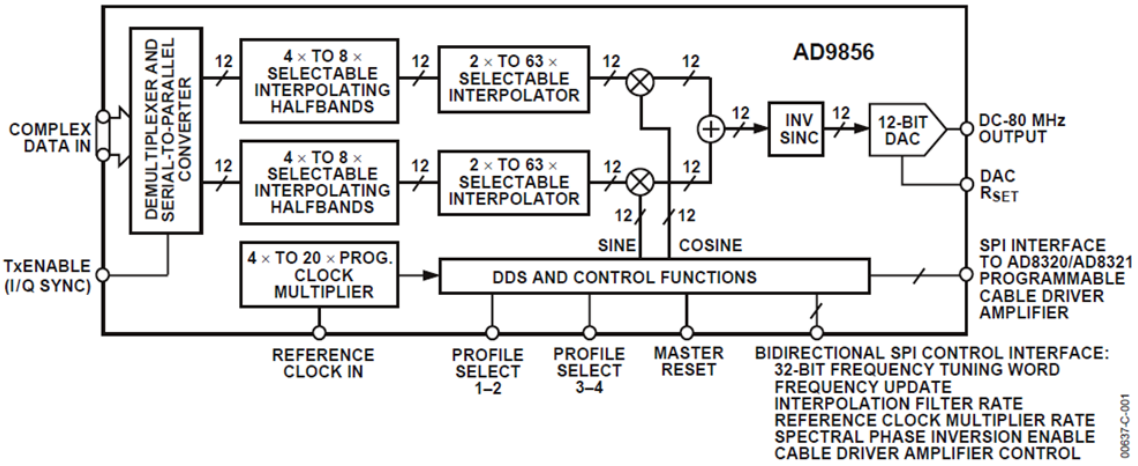

Figure 15: Functional Block Diagram of a Quadrature Digital Upconverter (Analog Devices AD9856)

For our chip, a 12-bit 200 Msamples/sec Segmented Current-Steering DAC is used to match the requirements of the system. The complete design is discussed in the next section.

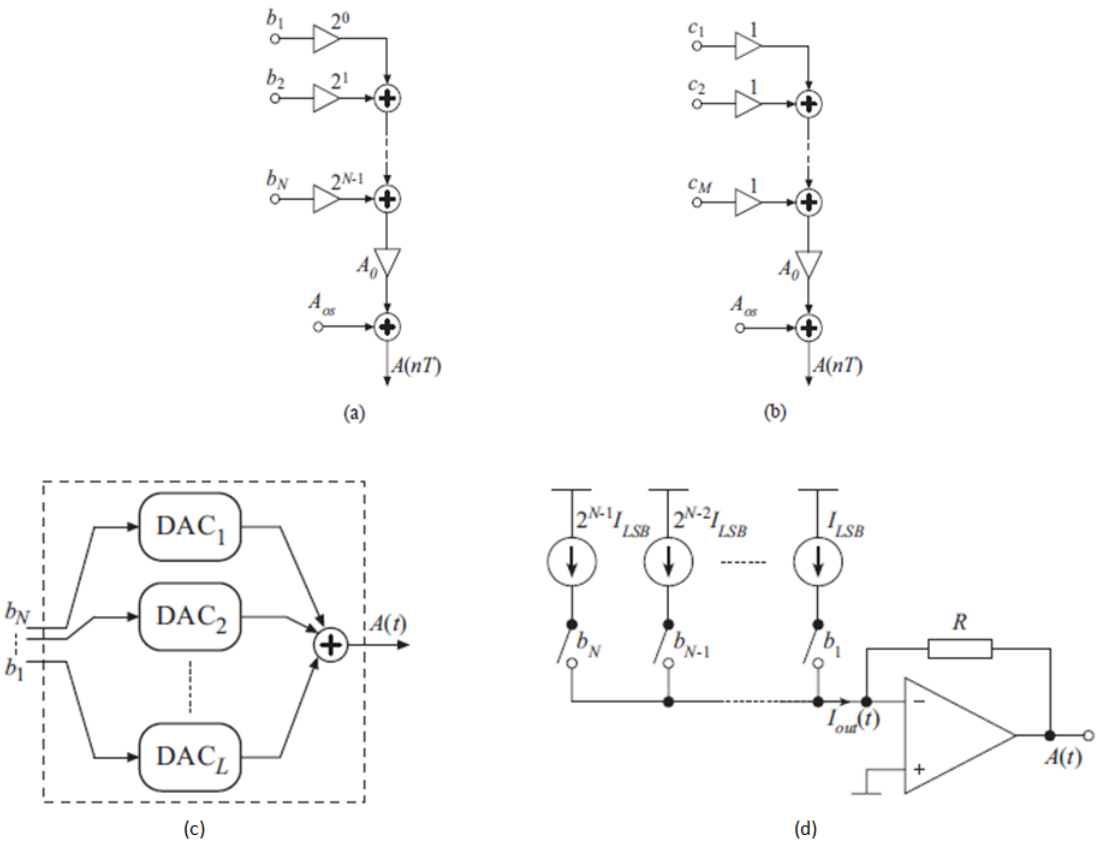

Figure 16: Different Architectures and Implementations. (a) Binary Weighted, (b) Thermometer-coded, (c) Hybrid Architecture, and (d) Current-Steering DAC

5 IMPLEMENTED ARCHITECTURE

In this section, we are going to discuss the architecture of the proposed DAC, segmentation ratio, and the evaluation of INL, DNL, mismatch error, and sizes of the transistors.

5.1 Segmentation Ratio

As mentioned in the introduction, a 12-bit 200 Msamples/s Segmented Current-Steering DAC is used. Figure 17 shows the architecture of segmented DACs. The design is composed of two main DACs, first, the Fine DAC, which is based on binary weighted current sources and these sources are controlled with the LSB bits of the input code. Second, the Coarse DAC, which is based on thermometer, coded inputs. The MSB of the input code is first encoded into thermometer code, and then fed to the thermometer coded DAC produce the output. The current from each DAC is then added to produce the total output current.

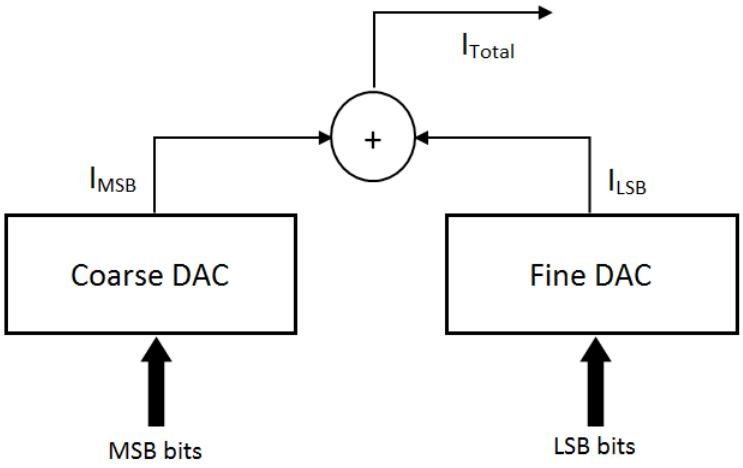

Figure 17: Architecture of segmented DACs

However, one of the important design parameters is how many bits will be assigned for the Fine DAC and how many for the Coarse. To answer this question we need to know some basics first. Table 12 shows the INL and DNL for different architectures where σ is the offset mismatch between current sources. This σ equals (for a simple current mirror)

$$\sigma = \frac{2A_{vt}}{V_{eff} \times \sqrt{WL}}$$

$$Area\ \alpha\ \frac{1}{\sigma^2}$$

Where A_{vt} is a technology dependent parameter.

Table 13: INL and DNL (in LSB) for different architectures

	Thermometer-Coded	Segmented	Binary-Weighted
σ_{INL}	$\frac{1}{2}\sigma\sqrt{2^B}$		
σ_{DNL}	σ	$\sigma\sqrt{2^{B_b+1}-1}$	$\sigma\sqrt{2^B-1}$

Where B is the no. of total bits, and B_b is the no. of bits used for binary weighted DAC. It is obvious thatσ_{DNL} gets worst as we move from left to right. Now suppose that we want DNL of 0.5 LSB for Thermometer-Coded architecture and A_{unit} is the minimum needed area for this requirement. From Table 12, we would need 4096 A_{unit}. However, same area would give the same performance in both. Some of different requirements are summarized in Table 13.

Table 14: Some requirements on INL and DNL, and their corresponding area

	Thermometer-Coded	Binary-Weighted
Area(INL = 0.5 LSB)	1024 A_{unit}	1024 A_{unit}
Area(INL = 1 LSB)	256 A_{unit}	256 A_{unit}
Area(DNL = 0.5 LSB)	A_{unit}	4096 A_{unit}

Therefore, to use the great advantages of Thermometer-Coded DACs and have a small area at the same time, a segmentation is need. The MSBs is encoded in Thermometer code where accuracy is needed the most and the LSBs is encoded in binary. Figure 18 shows a graph used to determine the optimum segmentation ratio. We will refer to a fully Binary-Weighted design as 0% and a fully Thermometer-Coded design as 100%.

The red line here represents the total analog area needed for Binary-Weighted DAC (0%) or Thermometer-Coded DAC (100%). The blue and green lines represent the total area needed for INL of 1 LSB and 0.5 LSB respectively. The grey line represent the area of the digital part (area for the encoders used to encode binary to thermometer coding).

The black line represent the area required for a total DNL of 0.5 LSB and a total INL of 1 LSB. Any point on that line satisfies the previous requirements, however, the horizontal line represent the minimum area needed to achieve these requirements. The point named Optimal Point is chosen because it represent the maximum segmentation ratio, which improves the total harmonic distortion due to glitches, and minimizes the DNL as well. It is about 53 % segmentation and we have 6 bits for the fine DAC and 6 bits for the Coarse DAC.

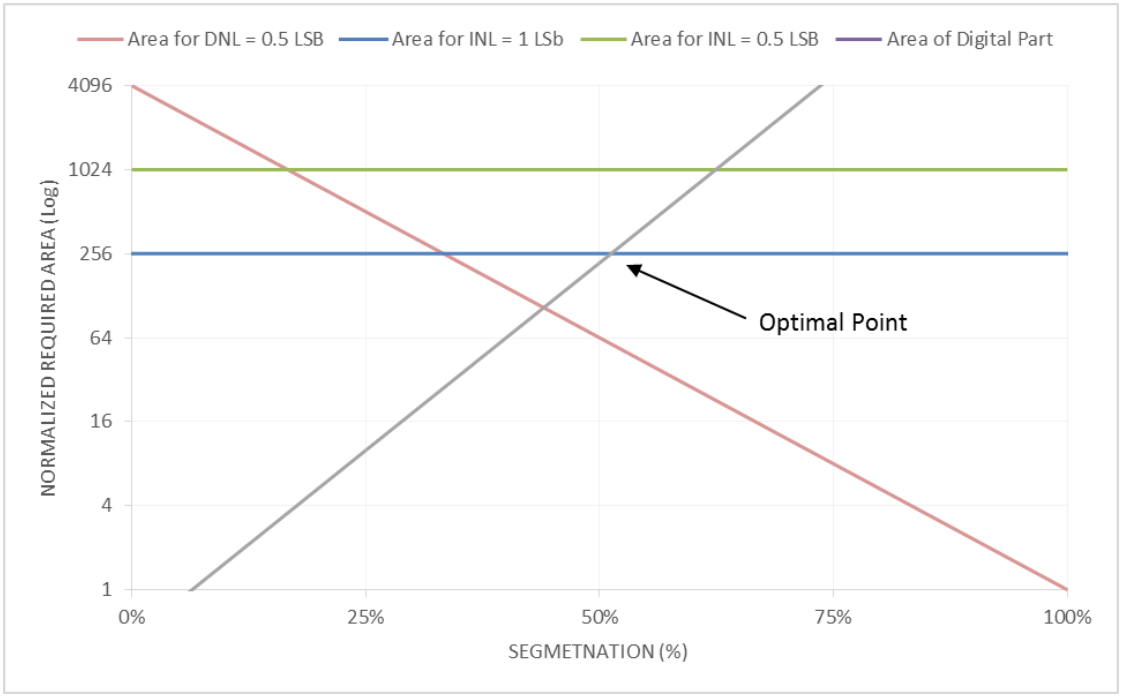

Figure 18: Normalized Required Area versus Percent Segmetnation

The black line represent the area required for a total DNL of 0.5 LSB and a total INL of 1 LSB. Any point on that line satisfies the previous requirements, however, the horizontal line represent the minimum area needed to achieve these requirements. The point named Optimal Point is chosen because it represent the maximum segmentation ratio, which improves the total harmonic distortion due to glitches, and minimizes the DNL as well. It is about 53 % segmentation and we have 6 bits for the fine DAC and 6 bits for the Coarse DAC. Next, we are going to discuss the building blocks of the DAC along with the desired specs.

5.2 Unit Cell

The basic building block of the DAC is the Unit Cell, which is shown in Figure 19. This cell architecture is used for both the Coarse and fine DACs. The transistor Q4 is connected in a simple current mirror circuit, the current passing through it the weighting element and is adjusted as desired. Its size is changed according to the position of the cell in the DAC (least

cell, first cell, etc...). Q3 is a cascaded transistor to increase Rout of the cell and biased with a voltage source. Both Q1 and Q2 acts as switches to steer the current left or right according to the input signal. This current is taken through resistors connected to VDD to get the output signal. As we see, a differential unit cell is used to guarantee large output swing, small area, and speed. The input of the switching transistors are the input and its complement, such that only one transistors is working at a time.

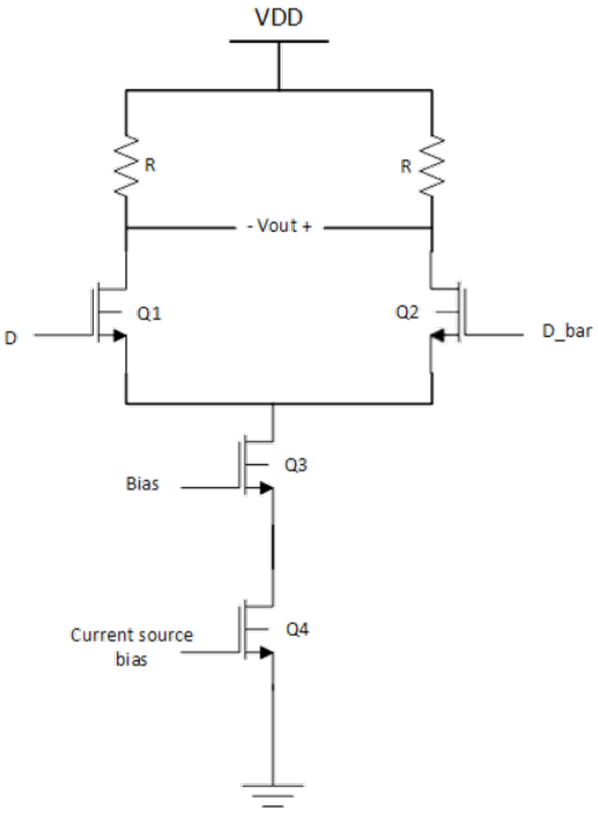

Figure 19: Basic Unit Cell

The transistor Q4 is connected in a simple current mirror circuit, the current passing through it the weighting element and is adjusted as desired. Its size is changed according to the position of the cell in the DAC (least cell, first cell, etc...). Q3 is a cascaded transistor to increase Rout of the cell and biased with a voltage source. Both Q1 and Q2 acts as switches to steer the current left or right according to the input signal. This current is taken through resistors connected to VDD to get the output signal. As we see, a differential unit cell is used to guarantee large output swing, small area, and speed. The input of the switching transistors are the input and its complement, such that only one transistors is working at a time.

5.3 Latch

The latch is the circuit used to drive the Unit Cell. It latches the input on the edge of the clock and holds it until the next edge. The latch is shown in Figure 20.

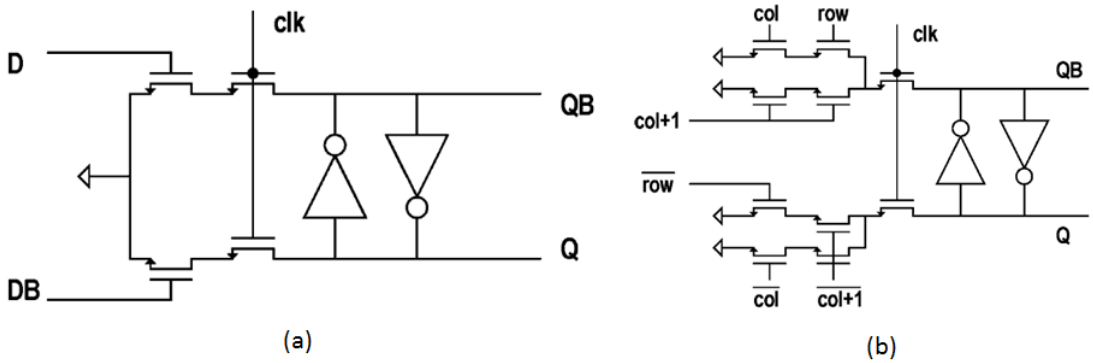

Figure 20: (a) latch for Fine DAC, (b) Latch for Coarse DAC

5.4 Decoders

The Coarse DAC is layouted in an 8x8 square matrix form. As shown in figure 21, two decoders are used to decode the input binary signal to thermometer-coded signal. This layout decreases the area required for the decoding logic and makes it easier to be layouted.

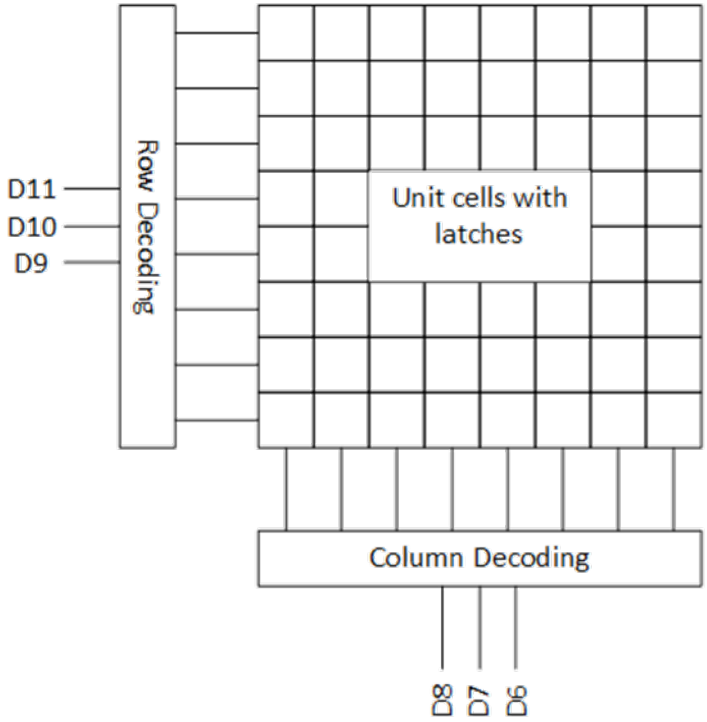

Figure 21: Coarse DAC

Table 14 shows the truth table of the encoder and is followed by its equations.

Table 15: Truth table of the encoders

A B C	R_1	R_2	R_3	R_4	R_5	R_6	R_7
0 0 0	0	0	0	0	0	0	0
0 0 1	1	0	0	0	0	0	0
0 1 0	1	1	0	0	0	0	0
0 1 1	1	1	1	0	0	0	0
1 0 0	1	1	1	1	0	0	0
1 0 1	1	1	1	1	1	0	0
1 1 0	1	1	1	1	1	1	0
1 1 1	1	1	1	1	1	1	1

$$R_1 = A + B + C \qquad R_5 = A(B + C)$$
$$R_2 = A + B \qquad R_6 = AB$$
$$R_3 = A + BC \qquad R_7 = ABC$$
$$R_4 = A$$

5.5 The Full DAC Architecture

The full DAC architecture is shown in Figure 22.

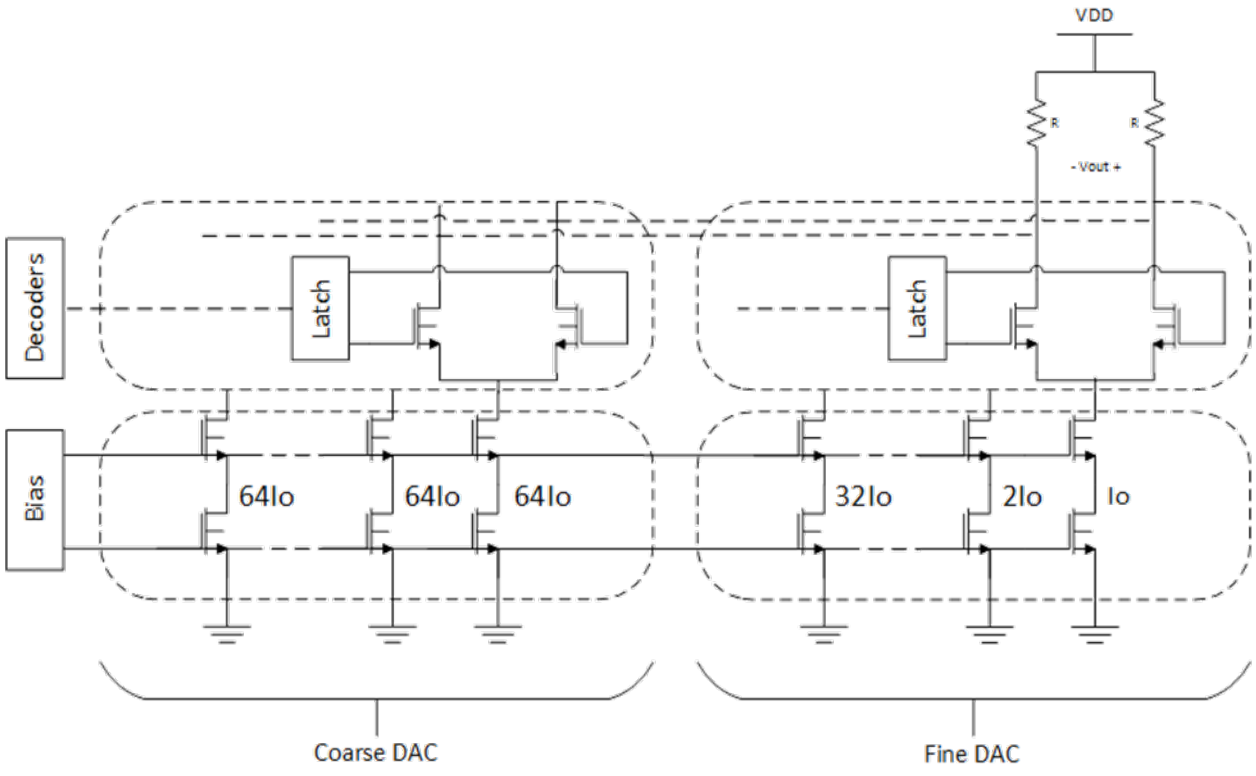

Figure 22: The Full DAC Architecture

The Coarse DAC is composed of 63 equally weighted current cells, while the Fine DAC is composed of six binary-weighted cells. Now, after getting the complete idea about the architecture of the desired DAC, we will move to specs need for the DAC. These specs is summarized in Table 15.

Table 16: DAC specification summary

OUTPUT SWING (DIFFERENTIALLY)	800 mV_{pp}
UPDATE FREQUENCY	200 MSamples/s
DNL	< 0.7 LSB
INL	< 1 LSB
VDD	1.2 V
R_L	50 Ω

In the next section, we are going to see the analysis to find out different design parameters (W/L, biasing voltage, etc...) which makes us achieve the aforementioned specs.

6 ANALYSIS

This section deals with the analysis and derivations of the different design parameters of the DAC. We will start by designing the current mirror to satisfy the INL requirements due to mismatches, followed by designing of the whole unit cell to satisfy the swing and the systematic INL and DNL.

6.1 Voltage Step and Io

As mentioned in Table 15, the output swing is $800mV_{pp}$. From Figure 19, it can be easily deduced that the voltage step is $2I_oR_L$ Where I_o is the current passing in transistor Q4. The factor of 2 comes from the fact that the output is differential. Now we can easily find the voltage step for Fine and Coarse DACs (will be referred to as LSB_{fine} and LSB_{coarse} respectively).

$$LSB_{Fine} = \frac{800\ mV_{pp}}{2^{12}-1} = 195.36\ \mu V.$$

$$LSB_{Coarse} = 2^6 LSB_{Fine} = 12.503\ mV.$$

Next, Io can be found by (where $RL = 50\Omega$, as in Table 4)

$$LSB_{Fine} = 2I_oR_L \Rightarrow\ I_o = 1.9536\ \mu A.$$

I_0 here represent the LSB current of the fine DAC. All the other currents are just multiples of the one.

6.2 W/L for Current Mirror and Veff

As mentioned before, W/L and V_{eff} for the current mirror plays and important role in determining the offset mismatch. The governing equation is:

$$\sigma = \frac{2A_{vt}}{V_{eff} \times \sqrt{WL}}$$

Where for the used technology Avt = 10 mV. Now the INL is

$$\frac{1}{2}\sigma\sqrt{2^B}$$

And B = 12 in our design, and to achieve INL < 1 LSB, then

$$INL = \frac{1}{2}\sigma\sqrt{2^{12}} = 32\sigma < 1 \Rightarrow \sigma < 0.03125.$$

$$\sigma = \frac{20\ mV}{V_{eff} \times \sqrt{WL}} < 0.03125 \Rightarrow V_{eff} \times \sqrt{WL} > 640.$$

Here V_{eff} is in mV and $\sqrt{WL}$ is in µm2. We are free to choose the values to satisify the above condition; however, choosing V_{eff} to be small would increase the area too much.

As shown in Figure 23, this is a voltage distribution of V_{eff} for all the transistors. The transparent branch on the right side means that this branch is off (switch is off) and the current passes in the left branch (switch is on).

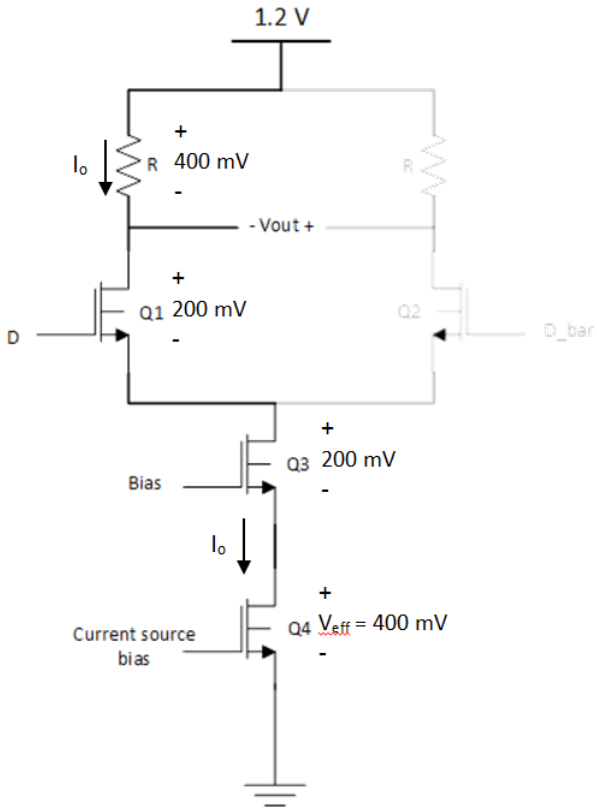

Figure 23: Unit cell with voltage distribution

To know how we get this distribution, imagine that the input code to the DAC is all ones, or in other words, all the current of all the unit elements will be steered to the left branch. With a simple calculation, one can find that the voltage drop across the resistor would be 400 mV. Therefore, we have 800 mV left out to be distributed over the three-cascaded transistors. Assume that we choose V_{eff} to be 400 mV; we have 400 mV left for the other two transistors. For WL of the current mirror, using V_{eff} = 400 mV, it is:

$$400 \times \sqrt{WL} > 640 \Rightarrow WL > 2.56.$$

6.3 Coarse DAC Systematic Mismatch

As shown in Figure 24, every unit cell is associated with R_o which in return will change the linearity of the DAC; however we can assure that the linearity wouldn't be altered much by choosing the right value for R_o.

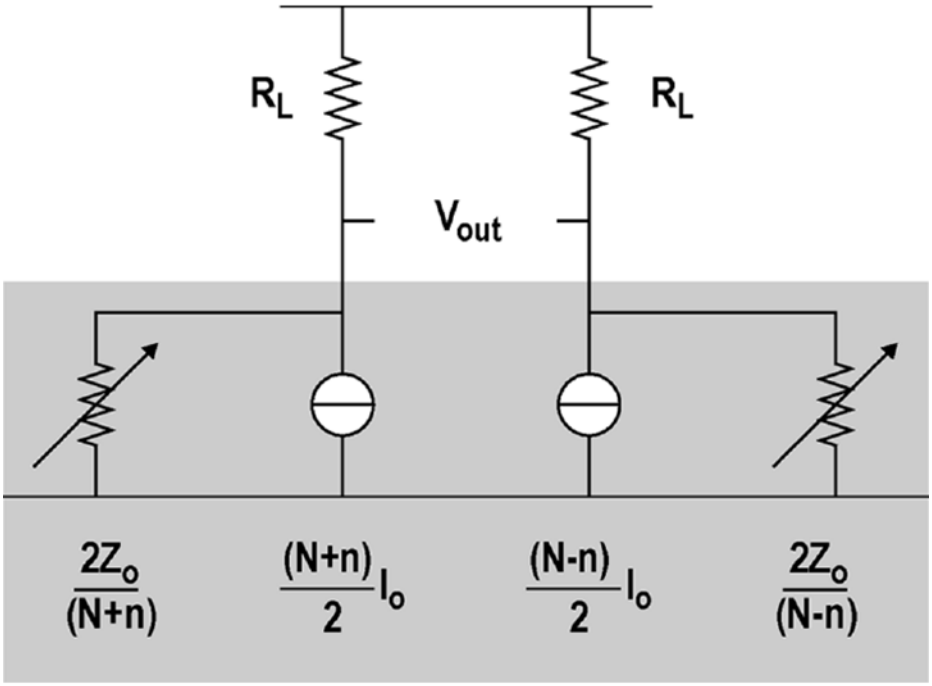

Figure 24: Effect of output resistance on DAC linearity

$Z_o$is the output resistance of the current source, Io is the value of one unit cell of the Coarse DAC, and n is the value of the input code, where –N $<$ n $\leq$ N. Depending on the input code, more or less current sources is connected to the left and right output nodes, and also more less output resistance will be in parallel with R_L. In the next equations, R_o will replace Z_o, and IC will replace I_o (so it won't be confused with Io of the Fine DAC).

$$V_{out} = R_L n I_c \left(1 + \left(\frac{nR_L}{2R_o}\right)^2\right)$$

To get the INL, we need to find V_{out} (ideal) first. It is represented by a straight line connecting the start and ending points of the above equation, these point are got by substituting n with –N and N respectively.

$$V_{out}(ideal) = R_L n I_c \left(1 + \left(\frac{NR_L}{2R_o}\right)^2\right).$$

$$INL = V_{out}(ideal) - V_{out} = \frac{I_c {R_L}^3}{4{R_o}^2}(n^3 - nN^2).$$

$$V_{out}(ideal) = R_L n I_c \left(1 + \left(\frac{NR_L}{2R_o}\right)^2\right).$$

$$INL = V_{out}(ideal) - V_{out} = \frac{I_c {R_L}^3}{4{R_o}^2}(n^3 - nN^2).$$

$$INL_{max} = \frac{2N^3 I_c {R_L}^3}{12\sqrt{3}{R_o}^2}.$$

Since $I^c = 2^6 I_o$, and $LSB_{Fine} = 2I_o R_L$, then

$$INL_{max}(LSB_{Fine}) = \frac{2^6 N^3 {R_L}^2}{12\sqrt{3}{R_o}^2}.$$

$$\frac{2^6 N^3 {R_L}^2}{12\sqrt{3}{R_o}^2} < 1 \Rightarrow R_o > 15.882\ k\Omega.$$

Table 16 summarizes the important design parameters that we deduced.

Table 17: Important design parameters

LSB_{FINE}	195.36 µV
LSB_{COARSE}	12.503 mV
I_O	1.9536 µA
V_{EFF} (current mirror)	400 mV
W/L (current mirror)	0.435µ/7µ
R_O	> 15.882 kΩ

Part III
Frequency Synthesizer

7 INTRODUCTION

The frequency band of operation is similar to the Digital TV (DTV) frequency band. There are many challenges in designing such applications, particularly in the design of the frequency synthesizer. The first and the most difficult one is the wide tuning range. synthesizer needs to cover from 30MHz to 1GHz to generate the required local oscillation (LO) signal, which means that it must have a tuning range larger than 200%. The second challenge is the phase noise requirement. Because of the wide tuning range, the voltage-controlled oscillator (VCO) in the frequency synthesizer needs to have a very large VCO gain(KVCO)and, thus, becomes sensitive to the noise voltage on the control line. The third challenge is the variations of the PLL loop dynamics and phase-noise performance. In a charge-pump PLL, the loop bandwidth is proportional to Kvco/N, the lock time is proportional to √(Kvco/N) , and the integrated phase noise is inversely proportional to Kvco/N , in which N is the PLL's total division ratio. For the reasons described above, minimizing the Kvco and fstep variations is required in a wideband LC VCO. It is hard to fulfill all these frequency resolution requirements in an integer-N phase-locked loop (PLL), unless a small reference frequency is used. However, narrow channel spacing leads to large division ratio that inevitably raises the in-band phase noise. The most popular way to resolve these problems is by using two or three VCOs and complex LO frequency generation techniques to cover the wide frequency range. Nevertheless, doing so not only draws more power but also increases chip area, which is not a satisfactory solution. In our work, we are working on a single-VCO fractional-N frequency synthesizer to cover all the required band. The fractional-N structure should also relieve the tradeoff between the phase noise and the step size, which allows us to use reference sources with higher frequencies, and thus, the inband phase noise can be reduced. To have a better phase noise performance and a wide tuning range, an inductor-capacitance-VCO (LC-VCO) is designed to oscillate at several gigahertz and divided by a programmable band-selecting divider to generate the required frequency. The frequency planning will be developed according to the tuning range and channels spacing, hence determine the modulus needed for the band-selecting divider.

8 FREQUENCY SYNTHESIZER

The block diagram of a PLL operating as a frequency synthesizer is shown in the following Figure. It consists of a reference oscillator (OSC), a phase/frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage-controlled oscillator (VCO), and two frequency dividers (FDs). The PLL is a feedback loop that, when in lock, forces ffb to be equal to fref. Given an input frequency fin, the frequency at the output of the PLL is

$$f_{\text{out}} = \frac{N}{M} f_{\text{in}}$$

where M is the divide ratio of the input frequency divider, and N is the divide ratio of the feedback divider. By choosing the frequency divide ratios and the input frequency appropriately, the synthesizer generates an output signal at the desired frequency that inherits the long-term stability of the input oscillator. In RF transceivers, this architecture is commonly used to generate the local oscillator (LO) at a programmable frequency that tunes the transceiver to the desired channel by adjusting the value of N.

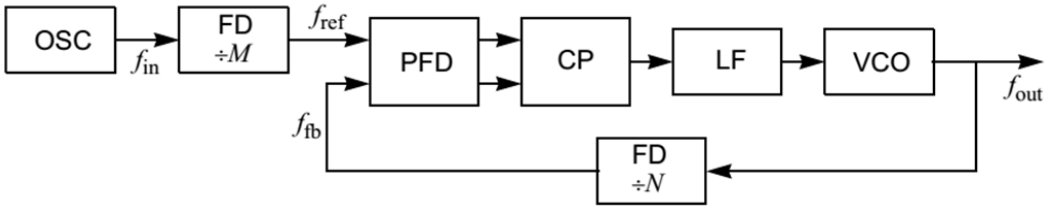

Figure 25: Typical Frequency Synthesizer Architecture

9 PLL MACROMODEL

The importance of building a behavioral macromodel is to assign specs for individual blocks through this system simulation and determine the weight of each block contribution in the system specs e.g. phase noise and settling time of the whole system and hence budgeting of specs. The phase noise macromodel is not optimized yet. It is used for system simulation after building all the transistor-level blocks. The direct noise simulation will consume a large time and may not converge so we need to build a phase noise behavioral model and extract some parameters that will be used in building the model blocks after simulating the noise of each block individually. The process of predicting the phase noise of a PLL using phase-noise models involves:

1. Using Spectre RF to predict the noise of the individual blocks that make up the PLL.
2. Building high-level behavioral models of each of the blocks that exhibit phase noise.
3. Assembling the blocks into a model of the PLL.
4. Simulating the PLL to find the phase noise of the overall system.

Concerning the simulation of loop dynamics, there are two different approaches to modeling PLLs. One approach is to formulate the models in terms of the phase of the signals, producing what are referred to as phase-domain models. In the simplest case, these models are linear and analyzed easily in the frequency domain, making it simple to use the model to predict phase noise, even in the presence of flicker noise or other noise sources that are difficult to model in the time domain. The other approach formulates the models in terms of voltage, and so are referred to as voltage-domain models. The advantage of voltage-domain models is that they can be refined to implementation. In other words, as the design process transitions to being more of a verification process, the abstract behavioral models initially used can be replaced with detailed gate- or transistor-level models in order to verify the PLL as implemented. Voltage-domain models are strongly nonlinear. Generally, the phase-domain models are considerably more efficient, but the voltage-domain models do a better job of capturing the details of the behavior of the loop, details such as the signal capture and escape processes. The phase domain models can be made more general by making them nonlinear and by analyzing them in the time domain. It is common to use such models with fractional-N synthesizers. Conversely, simplifications can be made to the voltage-domain models to make to them more efficient. It is even possible to use both voltage- and phase-domain models for different parts of the same loop. One might do so to retain as much efficiency as possible while allowing part of the design to be refined to implementation level. In general it is best to understand both approaches well, and use ideas from both to construct the most appropriate approach for your particular situation.

10 MODELS IN THE PLL LIBRARY

The PLL library includes the following voltage-domain models:

- Three-state digital phase frequency detector (PFD)
- Charge pump (current source version)
- VCO tuning curve (analytic and tabular versions)
- Frequency divider

10.1 VCO

- The VCO is modeled by its tuning curve. The tuning curve characterizes the relationship between the input voltage and the output frequency. The input to the VCO model is the loop filter output voltage, also called the VCO control voltage. The VCO output is a voltage representing the VCO's instantaneous frequency in Mhz. Therefore, when the VCO operates at 2 MHz, the model output is 2 Volts.
- The VCO tuning curve is generally nonlinear and can be specified in one of two ways:
  - With the coefficients of a fourth order polynomial
  - With a look-up table
- VCO - Polynomial tuning curve:

The input voltage is internally clamped to the nearest end point if it moves outside the interval [*min-vco-input-voltage*, *max-vco-input-voltage*]. Although the input voltage may fall outside the interval, the output behaves as though the input voltage value is at the end points. Within the interval, the output is a fourth order polynomial in the quantity, Vinput minus the free running voltage. When the input voltage equals the free running voltage, the output frequency equals the free running frequency. The scale factor scales the entire polynomial and has a default value of 1. The scale factor is useful in converting data in KHz/volt, for example, to the required MHz/volt. The parameters are the coefficients of the Polynomial.

- VCO - Table look-up tuning curve:

The two parameters are the scale factor and the path to the look-up data. The look-up model linearly interpolates between data points and linearly extrapolates outside the data interval. The data format is two columns of data delimited by spaces. There is no header, and there are no extra lines at the end. The first column is input voltage. The second column is output frequency.

10.2 Frequency Divider

The frequency divider is essentially a simple gain element. It takes an input voltage that represents frequency in Mhz, and then scales it by the divide ratio to generate an output voltage that represents the divided frequency. The divide ratio is numerically equal to the voltage on the control pin. If the divide ratio drops below 0.001, the model assigns it to 0.001 and issues a warning. This assignment prevents division by zero during simulation.

10.3 Charge Pump

The charge pump transforms the duty cycle into the expected average current sourced or sunk by the charge pump. You define the maximum source and sink currents, and they can be different from each other. If the charge pump output voltage exceeds the rails you define, the output voltage is clamped to the rail through a 0.001 Ohm resistance. The other parameters are the leakage resistance and open circuit voltage. These last two parameters specify the Thevenin equivalent circuit of a leakage path. The leakage path can source or sink current depending on the open circuit voltage.

10.4 Loop Filter

The loop filter is added one component at a time.

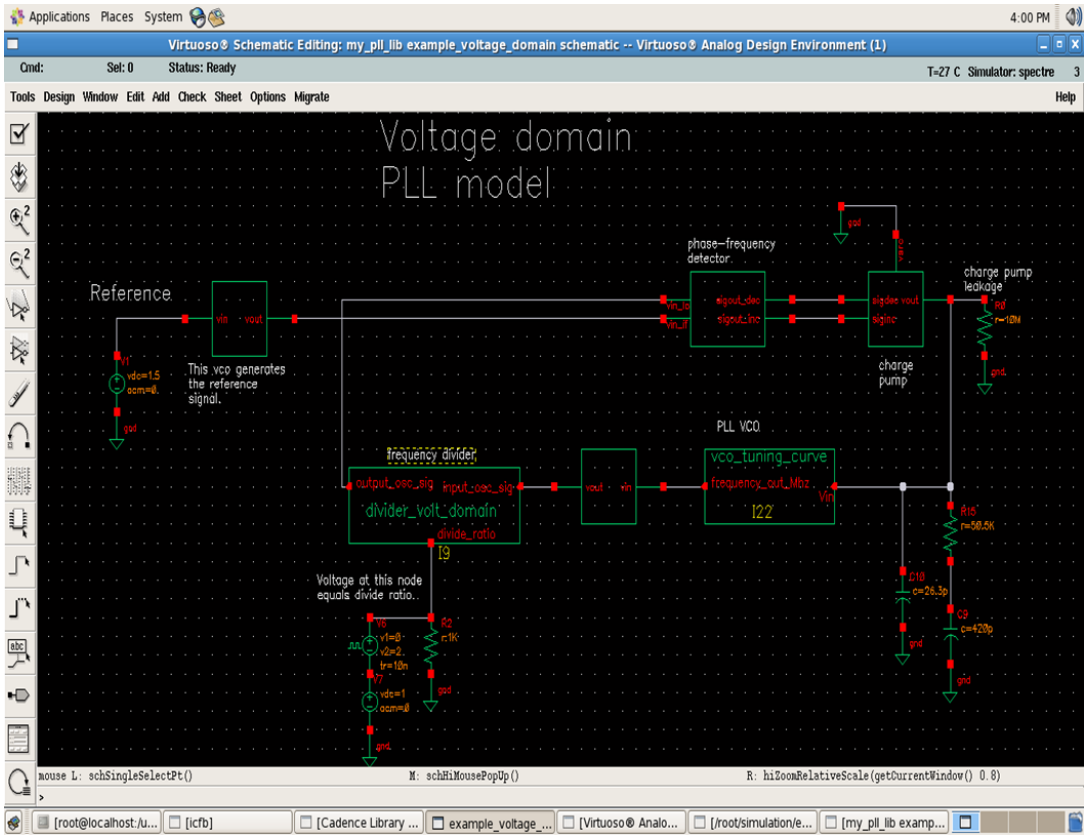

Figure 26: Macromodel snapshot

11 SYSTEM LEVEL DESIGN PROCEDURE AND SIMULATIONS

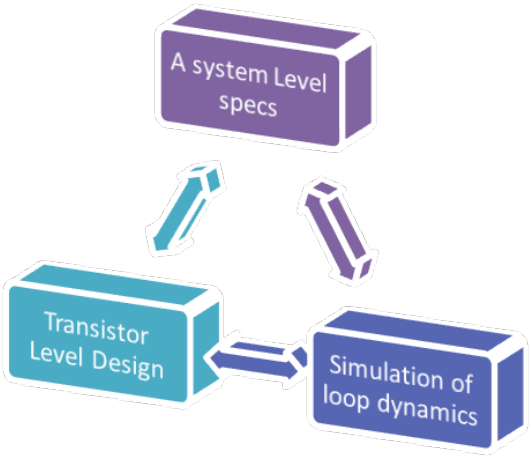

Figure 27: System design methodology

A Summary of PLL design trade-offs is shown in Table 17:

Table 18: PLL design tradeoffs

	Loop bandwidth	Damping
Faster settling	wide	under
Better stability	narrow	over
Lower phase noise	wide	N/A
Better spur rejection	narrow	N/A
Low jitter peaking	N/A	over
Low overshoot	N/A	over
Smaller capacitor size	wide	N/A

System Level design parameters

- Charge current pump (Imax)
- Loop filter components (R1,R2,C)
- VCO Tuning range and Free running frequency
- VCO gain (Kvco)
- Loop Division factor (N)

11.1 GSM Cellular Communication PLL Example

It is required to synthesize 890 to 960MHz with a resolution of 200kHz using a power supply of 2.7V

Step 1: Determine VCO Tuning Range:

- The maximum and minimum output frequencies determine the PLL frequency range.
- This is the range of frequencies under which the PLL is operating. The frequency range for this PLL is 890 to 960MHz. This requires that the VCO have a tuning range at least 890 to 960MHz. VCO Tuning Range = 890 - 960MHz

Step 2: Determine Loop Division Ratio Range:

- This is determined by the synthesizer's frequency resolution. Here the frequency resolution is the channel spacing of 200kHz.
- If it is assumed that a 200kHz reference is used to achieve a 200kHz resolution (Fref = GCD (890M,0.2M) = 0.2M), N will have the following range. 4450 <N <4800
- The value of N has an effect on other loop parameters. Therefore, in defining the other parameters the geometric mean of N will be used

$$N_{mean} = \sqrt{N_{\min} N_{\max}} = 4622$$

Step 3: Determine Damping Factor ζ :
Damping factor, ζ has an effect on the speed and stability of the system. As a compromise between speed and stability, ζ is optimally set to the following value. $\zeta = 0.707$

Step 4: Determine Natural Frequency , w_n and the loop BW w_c:
Frequency has a significant effect on the loop bandwidth. For a charge pump PLL with a passive loop filter, the loop bandwidth, w_{3dBn}, is related to the natural frequency by the following:

$$\omega_{3dB} = \omega_n \left[2\zeta^2 + 1 + \sqrt{\left(2\zeta^2 + 1\right)^2 + 1} \right]^{1/2}$$

- If $\zeta = 0.707$ is assumed, this results in $w_{3dB} = 2.06 w_n$.
- It is desirable to make the loop bandwidth less than 1/10 of the input reference frequency (200kHz) in order to avoid the continuous time approximations of the charge pump PLL breaking down. However, it is desirable to make the loop bandwidth as wide as possible in order to suppress the VCO phase noise that is the dominant source of phase noise for the integrated PLLs.
- As a compromise between stability and noise performance, the loop bandwidth is set to the following:

$$\omega_{3dB} = \frac{\omega_{ref}}{10}(0.75) = 94.2 \, krad/s$$

- This results in the natural frequency equal to the following for$\zeta = 0.707$:

$$\omega_n = \frac{\omega_{3dB}}{2.06} = 45.8 \, krad/s$$

Step 5: Determine VCO Gain:

- The tuning range of the VCO and the VCO control voltage range set the VCO gain.
- From step 1 it was shown that the VCO needs to tune a minimum frequency range of 890 to 960MHz. The VCO control voltage range is limited by the power supply and the voltage levels necessary to keep the charge pump in saturation. The charge pump will no longer behave ideally if the VCO control voltage rises too high or falls too low.
- Therefore, the VCO control voltage is limited to a minimum of a DSAT V from the supply rails. With a power supply of 2.7V, a VCO control range of 1.6V can be assumed with sufficient margin to handle process variations. This results in the following VCO gain.

$$K_{VCO} = \frac{2\pi(960\text{MHz} - 890\text{MHz})}{1.6\text{V}} \frac{rad}{sV} = 275 \frac{Mrad}{sV}$$

Step 6: Determine Charge Pump Current and Loop Filter Capacitor:

- The charge pump current and the loop filter capacitor can be determined by the relationship between the natural frequency, the loop division factor, and the VCO gain.
- It is desirable to have a high charge pump current because this will result in a higher loop gain and thus a more stable system.
- However, having a large charge pump current will result in a large capacitor as shown:

$$C_1 = \frac{IK_{VCO}}{2\pi N \omega_n^2}$$

- A large capacitor will translate into increased circuit area.
- Therefore a design tradeoff between loop gain and silicon area arises. The charge pump current can be set so that it will result in a decent loop gain without producing too large of a capacitor as shown in the following:

$$\text{Set } I = 10\mu A$$
$$C_1 = \frac{(10\mu A)\left(275 \frac{Mrad}{sV}\right)}{2\pi(4622)\left(45.8 \frac{krad}{s}\right)^2} = 45.1pF$$

Step 7: Determine Other Loop Filter Components:

- The loop filter resistor is used to set the damping factor as shown in the following equation:

$$R = \frac{2\zeta}{\omega_n C_1} = \frac{2(0.707)}{\left(45.8 \frac{krad}{s}\right)(45.1pF)} = 685k\Omega$$

- The second loop filter capacitor, 2 C , used to suppress ripple in the control voltage is fixed to be less than a tenth of the main loop filter capacitor C1 so that the loop can still be considered a second order system.

$$C_2 < \frac{C_1}{10} = 4.51pF$$

Simulation results: Figures 28-32 show simulations results.

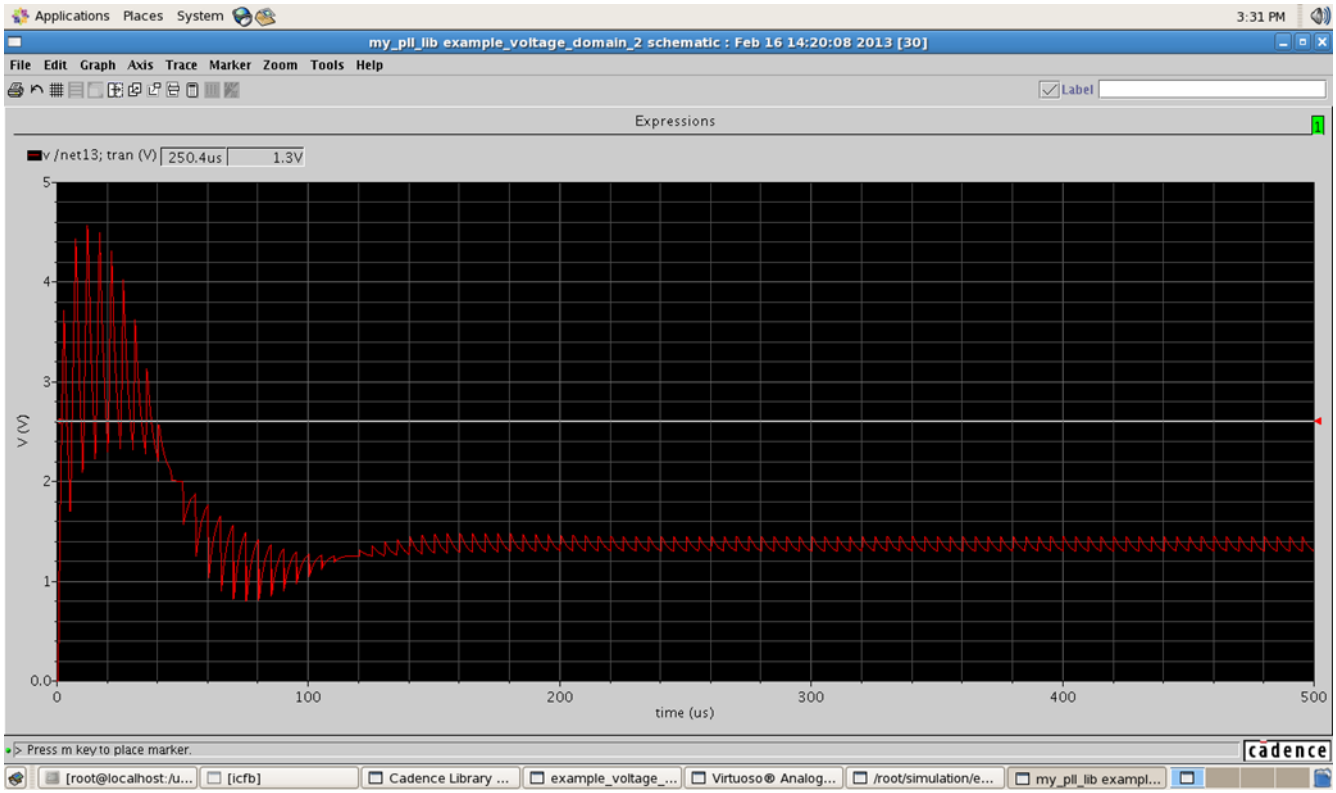

Figure 28: VCO control voltage

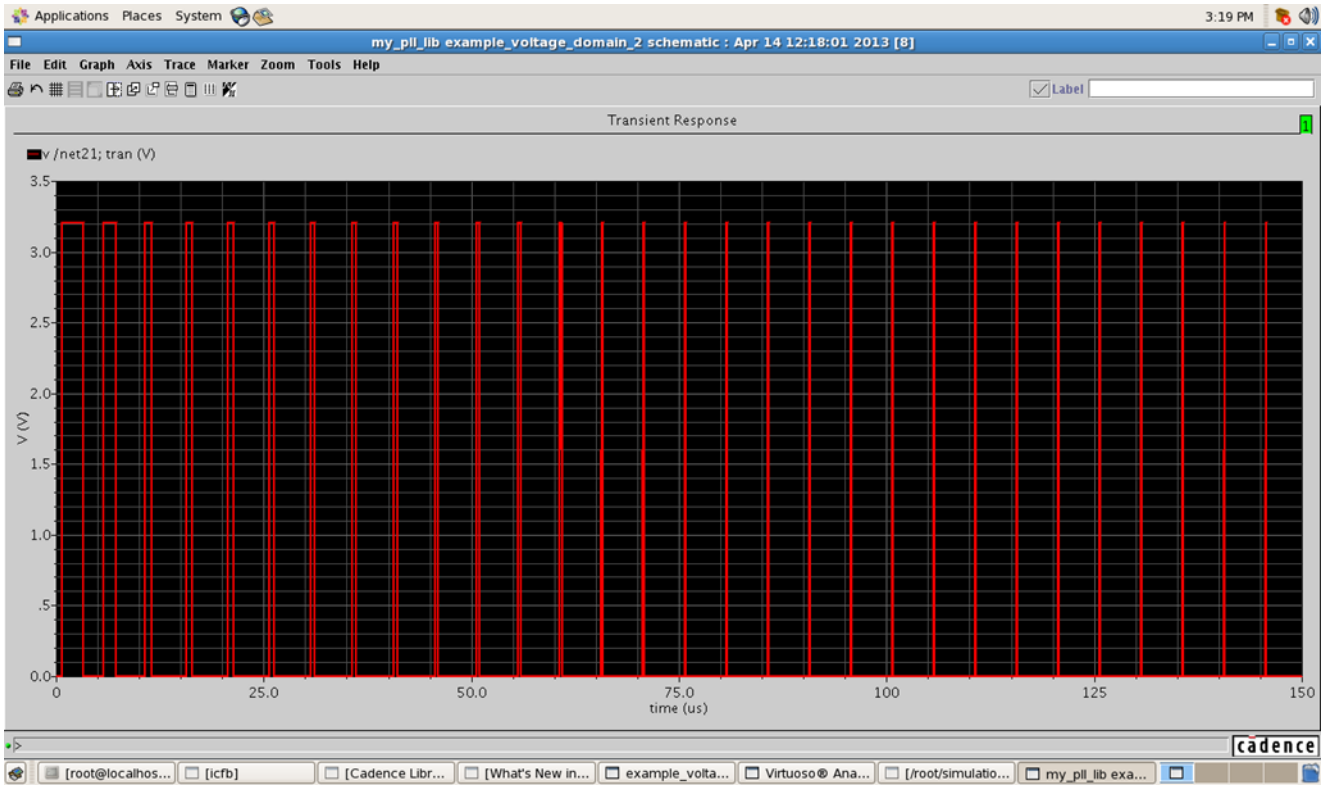

Figure 29: PFD output

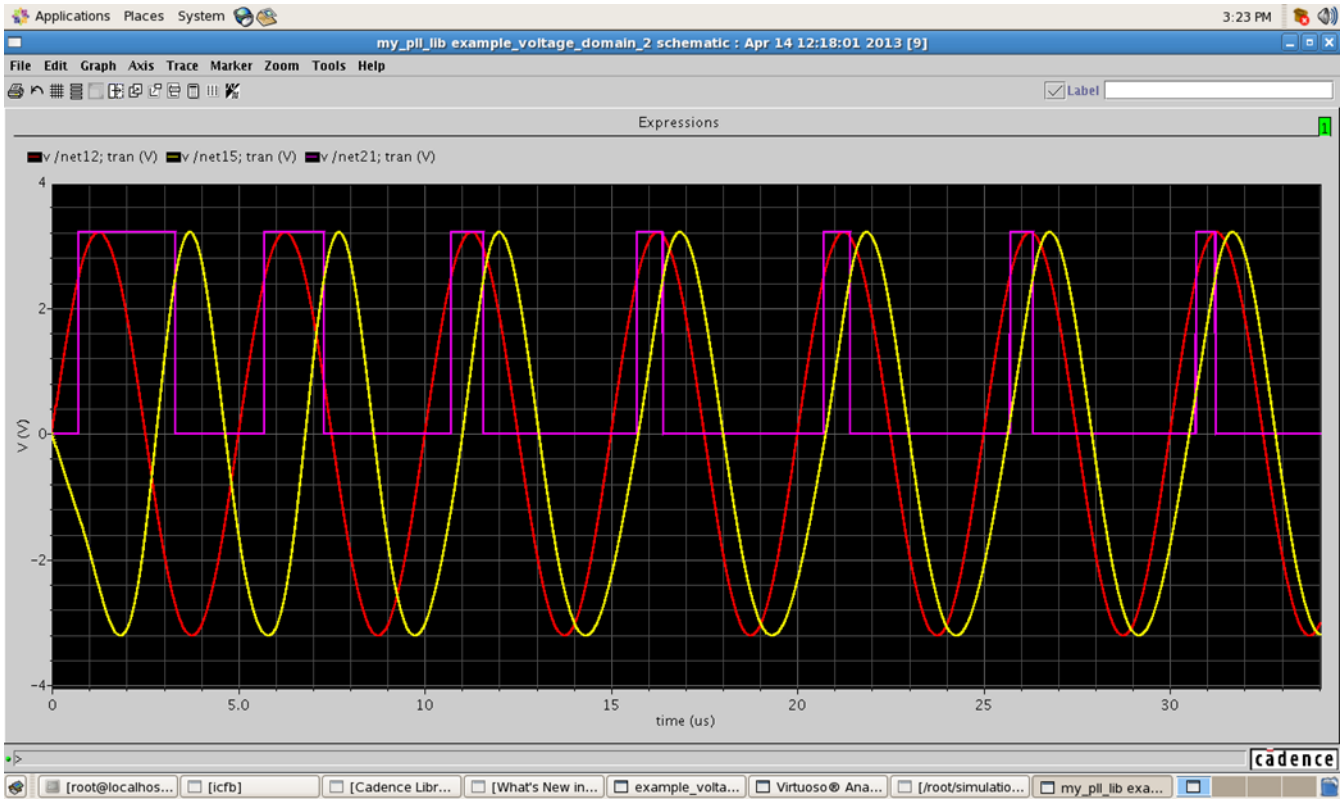

Figure 30: PFD inputs and output

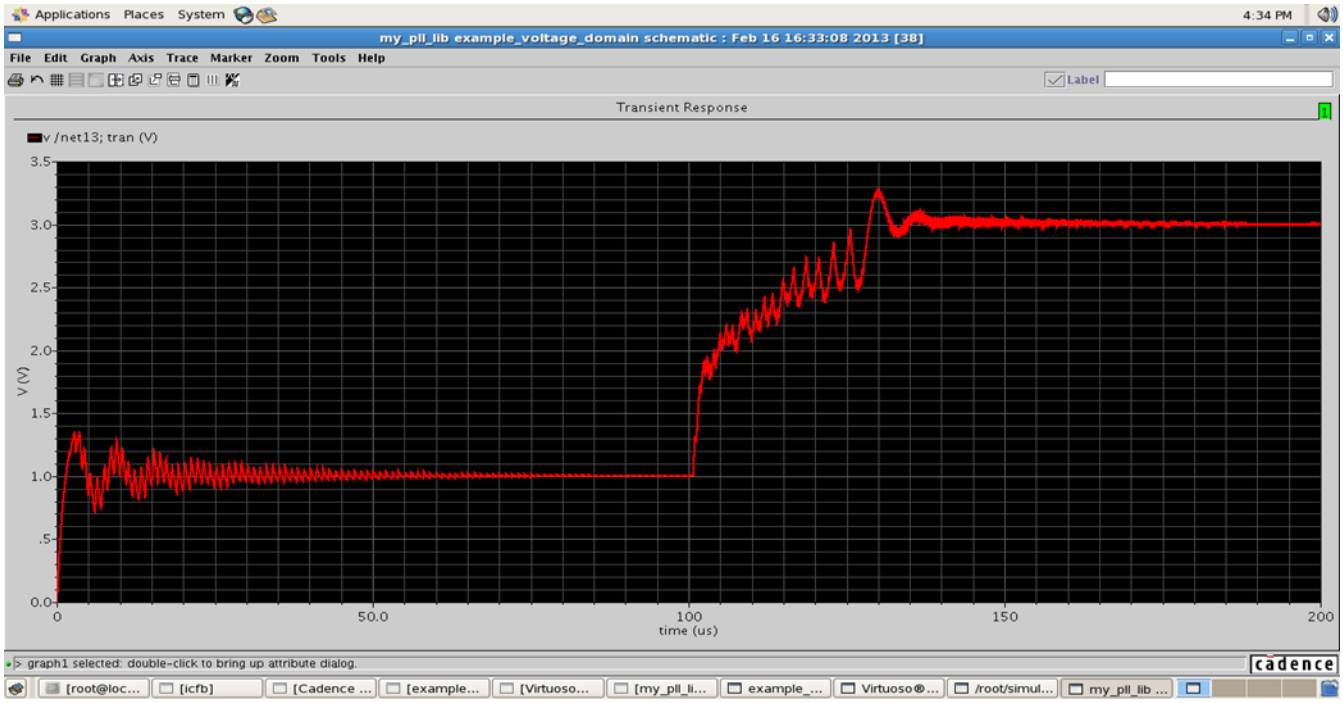

Figure 31: VCO control signal settling time

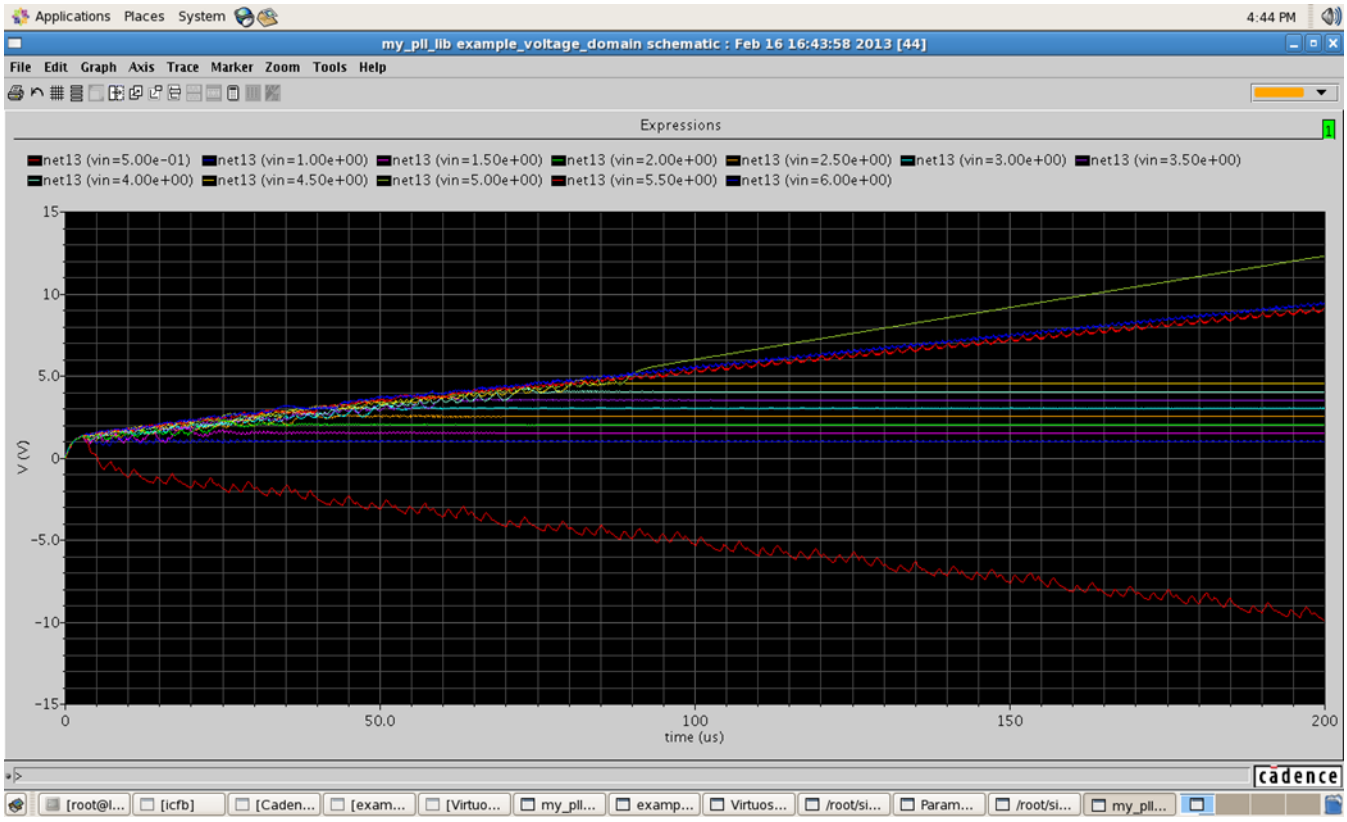

Figure 32: VCO control signal ranges

Conclusions:

- This design procedure has defined all the key system level parameters required to start the design.
- The next step in the circuit design is to construct a system level macro model which allows simulation of the loop dynamics.
- Then transistor level design is started.
- The design process is generally an iterative process. For example, non-idealities introduced by the transistors can be compensated by adjusting parameters in the system level macromodel and then translating those adjustments back to the transistor level.
- There are usually many design iterations involved in such a complex system level design as a PLL.

11.2 Circuit Implementation

11.2.1 System Architecture

The block diagram of the proposed frequency synthesizer is depicted in Figure 33. The main loop consists of a phase/frequency detector (PFD), a charge pump (CP), an off-chip loop filter (LPF), an LC-VCO with a 5-bit capacitors array, and a multimodulus divider (MMD). A $MASH-111\triangle-\Sigma modulator$ (DSM) is used to dither the modulus of the MMD to generate fractional division ratio. An auto-frequency calibration (AFC) loop is employed to automatically choose the coarse setting of the capacitors array. The band-selecting divider is connected to the output of the VCO to produce the desired output frequency. All the control signals

are sent into the on-chip registers through a three-wire interface control circuit (TWIF) with inputs of serial in (SI), load enable (LE), and clock (CLK).

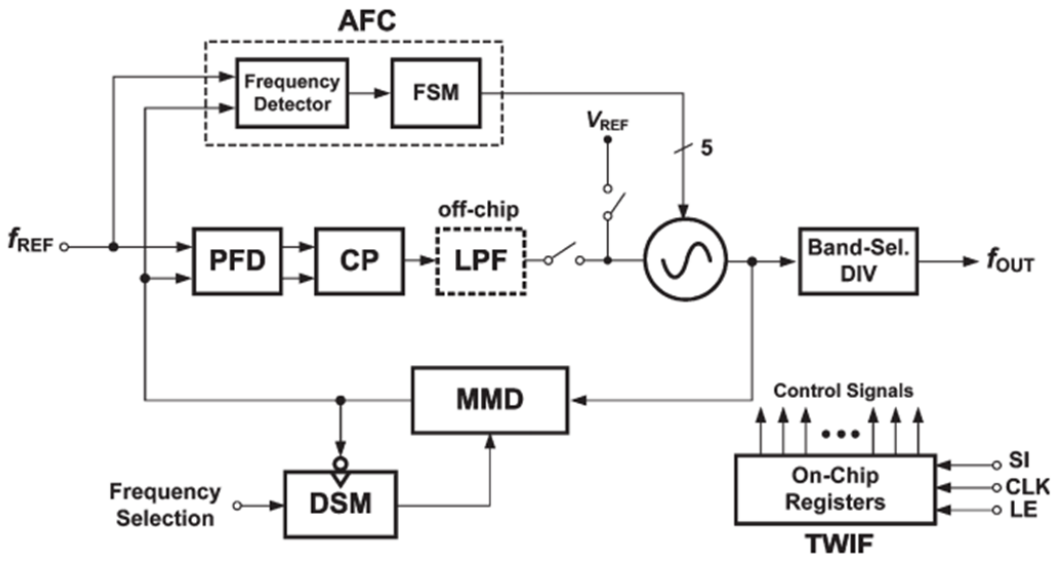

Figure 33: Implemented Frequency Synthesizer Architecture

11.2.2 VCO

The schematic of the LC-VCO is illustrated in Figure 34. Two complementary NMOS and PMOS are used to form the negative transconductance. The LC tank consists of a differential inductor and two PMOS varactors operated in the accumulation mode. The tail current source has been removed to improve the phase noise, because the tail current is the dominant source of flicker noise and the oscillation amplitude can thus be maximized to nearly full swing. On the other hand, this VCO will always operate in the voltage-limited regime along the entire tuning range and delivers more ideally constant amplitude. However, removing the tail current source makes the VCO sensitive to the voltage variation on the power line, which leads to a bad pushing figure of the VCO. This problem can be fixed by separating the voltage supply of the VCO from other circuit blocks and using a voltage regulator to regulate the supply voltage. Thus, the noise coupling through the power supply can be reduced. Since a wide frequency range from 2300 to 3900 MHz is required in this application, a 5-bit binary-weighted capacitors array is connected to the tank to extend the tuning range of the VCO and keep VCO gain (KVCO) small. To maintain a monotonic switching tuning characteristic, the capacitors array is laid out using a unit cell which consists of a metal–insulator–metal capacitor as well as a switching NMOS. The capacitance of the unit capacitor is 114 fF, and the size of the switching NMOS is $4\mu m/0.13\mu m$. The layout of the capacitors array is also arranged in a common-centroid configuration for better symmetry. The measured VCO frequency versus the tuning voltage as well as the digital control words of the capacitors array is shown in Figure 34. The VCO frequency has a tuning range of 2100 MHz from 2300 to 4400 MHz, which covers all the desired frequency bands, and the VCO gain is smaller than 140 MHz/V.

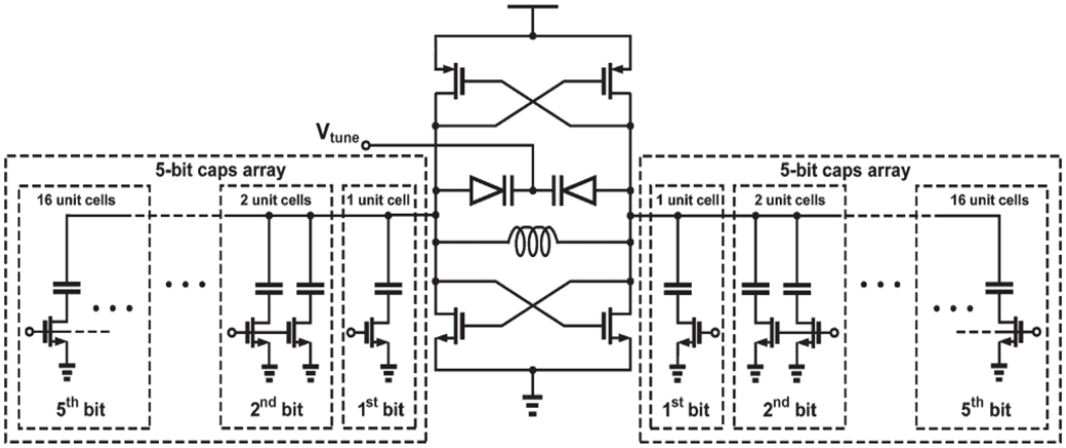

Figure 34: Digital Dual Quadrature Down-Conversion Structure

11.2.3 Dynamic AFC (DAFC) Loop

Because the VCO has a 5-bit capacitors array, the system needs an AFC loop to automatically choose the capacitors array setting whenever the output frequency of the synthesizer is changed. The AFC loop not only chooses the proper tuning curve for the PLL but also guarantees the VCO to operate at the center of the tuning curve, which makes the PLL operates with linear transfer characteristic and minimizes the mismatch of the up and down current of the charge pump. Note that the output dc voltage of the charge pump is usually designed to be at the middle of the tuning curve, and since the charge pump has a finite output impedance, operating the charge pump at high output voltage will decrease the up current as well as increase the down current and vice versa. This will degrade the linearity of the charge pump and lead to a higher spur. In addition, the AFC can also calibrate the VCO frequency error caused by variations of the process, temperature, and supply voltage. There are many ways to carry out an AFC loop. They can be roughly categorized into the following two groups: 1) the analog method and 2) the digital method according to their frequency detection technique. The analog method converts the frequency information into the voltage information and compares the frequency difference between the desired frequency and the current frequency by a voltage comparator. The analog methods usually have a benefit of fast settling since the frequency comparison can be quickly done in a few reference cycles, but their drawback is larger chip area as well as power consumption. In contrast, in digital methods, only digital circuits are used in frequency comparison; hence, the circuit area and the power consumption are much smaller than those in the analog methods, although it requires a longer frequency-detection time. Therefore, in our architecture, the digital method is adopted.

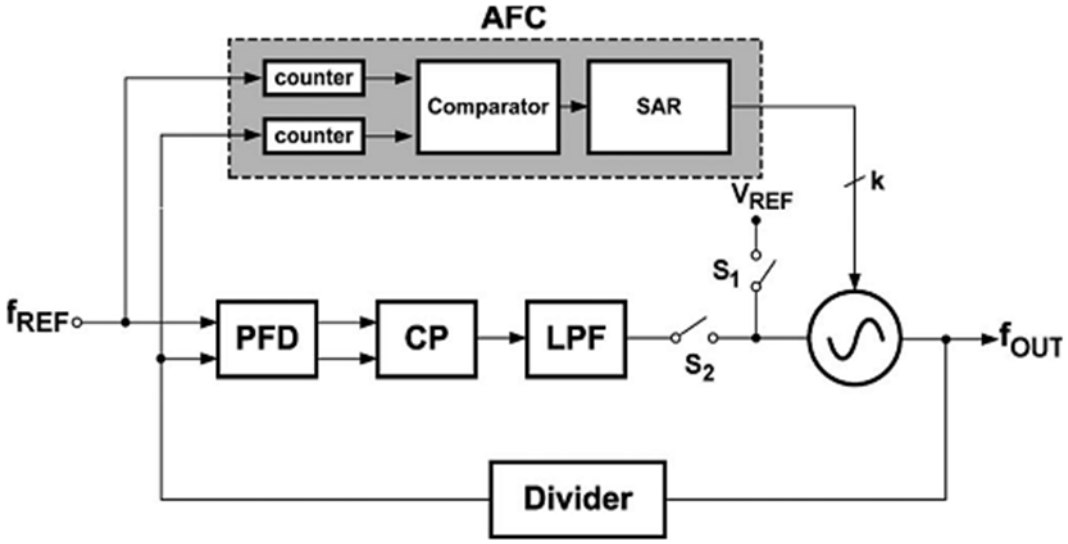

Figure 35: The block diagram of the conventional digital AFC

When the output frequency of the synthesizer is changed, the control voltage of the VCO is switched to a constant voltage VREF (S1 close, S2 open), and the AFC loop starts to search the proper setting of the capacitors array. After the coarse setting is decided, the control voltage of the VCO is switched back to the LPF (S1 open, S2 close), and the PLL starts to lock the phase of the VCO. The AFC loop utilizes two counters and a comparator as a frequency detector. The two counters count the input pulses of the reference signal and the divided-VCO signal in a specified time period (TAFC). By comparing the pulse numbers in these two counters, the frequency difference can easily be determined, and accordingly, the successive approximation register (SAR) can decide to increase or decrease the frequency of the VCO. The SAR uses the binary search algorithm to determine the final coarse setting of the VCO. Therefore, the same procedure repeats K times, where K is the bit number of the capacitors array. In this paper, since the VCO has a 5-bit capacitors array, the bit number of the SAR should be five, and thus, the total time for the AFC is 5*TAFC. The time period TAFC is an important parameter of the AFC technique. System designers want TAFC to be short so that the switching time of the frequency synthesizer can be minimized. However, TAFC is inversely proportional to the desired frequency resolution f_{RES} of the AFC. For example, if we are going to tell a frequency difference of 1 MHz, a $1\mu sec$ time period is a minimum value for TAFC. However, considering that the two input signals may not have aligned phases or the same starting points, TAFC has to be at least $2\mu sec$ long to make sure that the frequency difference can be correctly judged. A short TAFC makes f_{RES} large, which may result in a wrong setting of the capacitors array. As we mentioned before, the AFC takes K procedures to finish the coarse setting. In the conventional method, every procedure takes TAFC to settle, but actually, not every procedure needs that long time period, particularly when the frequency difference between the VCO frequency and the target frequency is much larger than f_{RES}. Therefore, the total AFC time can be reduced if the frequency judging time TAFC can be dynamically changed according to the frequency difference. We use a dynamic method to realize this DAFC.

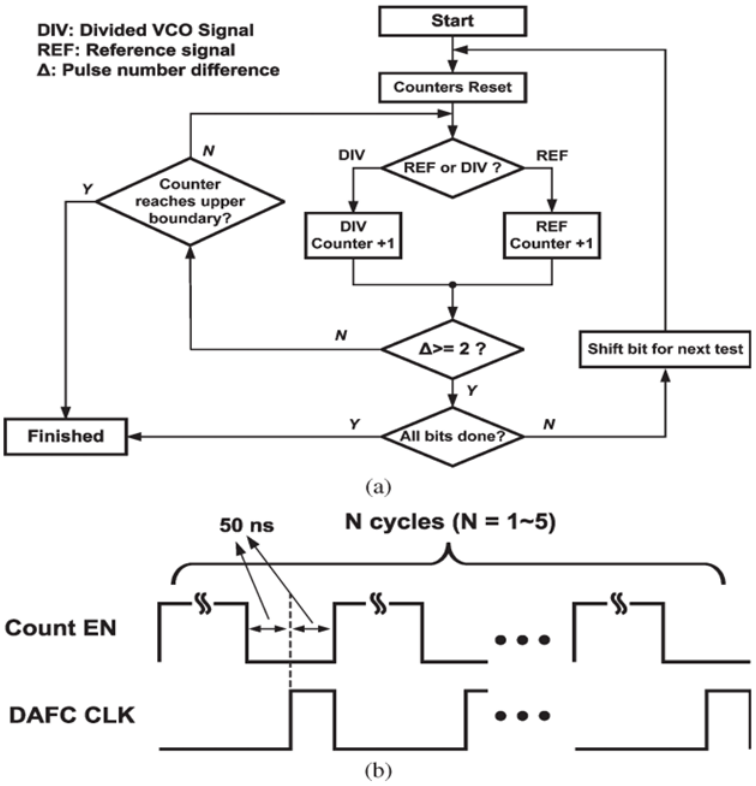

Figure 36: DAFC Flow Chart and Timing Sequence

The DAFC loop still uses two counters to count the pulses of the reference signal and the divided-VCO signal, but the judging of the frequency difference is repeated continuously whenever any of the two signals comes. As soon as the difference of the pulse numbers is greater than two, which signal is with higher frequency can be found, and then, the current DAFC procedure terminates, and the next DAFC procedure starts to determine the next bit. The number two is chosen so that the error caused by the different starting point can be avoided. Nevertheless, when the current setting makes the VCO frequency very close to the target frequency, the procedure may take a very long time to terminate, which may even be longer than conventional TAFC. To prevent this situation, an upper boundary is added in the DAFC process. When any one of the counters reaches this upper boundary, the process terminates, and the decision circuit chooses the current setting as the final results. The upper boundary determines the longest period of one DAFC procedure TDAFC, which is inversely proportional to the frequency resolution f_{RES} of DAFC. If we want the f_{RES} to be smaller than 1 MHz, TDAFC has to be at least $2\mu sec$. With a reference frequency of 40 MHz, the resulting upper boundary of the counting number is 80. To make the counter easier to implement, the counting number is chose to be a power of two, e.g., 128. In this paper, we choose our counting number to be 256, and the corresponding f_{RES} becomes 312.5 kHz ($= 2 \times 1/6.4\mu sec$). The total time required for the DAFC is not the same for different output frequencies. The shortest case takes only one cycle ($6.4\mu sec$) to finish if the desired output frequency is very close to our initial setting. The worst case happens when the DAFC has to take five procedures to finish. However, even in this case, the first two procedures must take very short time to finish because they are very far from the final frequency. Generally speaking, the DAFC can reduce the procedure by two cycles, or in other words, the DAFC time is about total_bits−2 cycles, which is $19.2\mu sec$ in this paper. In our experiment, the longest DAFC time is $22.2\mu sec$ among all channels. The timing sequence of the DAFC is illustrated in Figure 36(b). To avoid the counting error when the capacitors array is switched, we put the rising edge of DAFC clock

(the time when capacitors array is switched) in the middle of two successive counting processes [Count EN in Figure 36(b)]. The time between the DAFC clock and each counting process is about 50 nsec, while the VCO settling time is found to be smaller than 1 ns from simulation. Therefore, the space is enough to avoid the counting error when the capacitors array is switched.

Figure 37 shows the simulation results of the conventional AFC and the DAFC process. It can be seen that the conventional AFC process has the same period in determining every control word of the capacitors array, while the DAFC has a shorter period when the setting is far from the final goal.

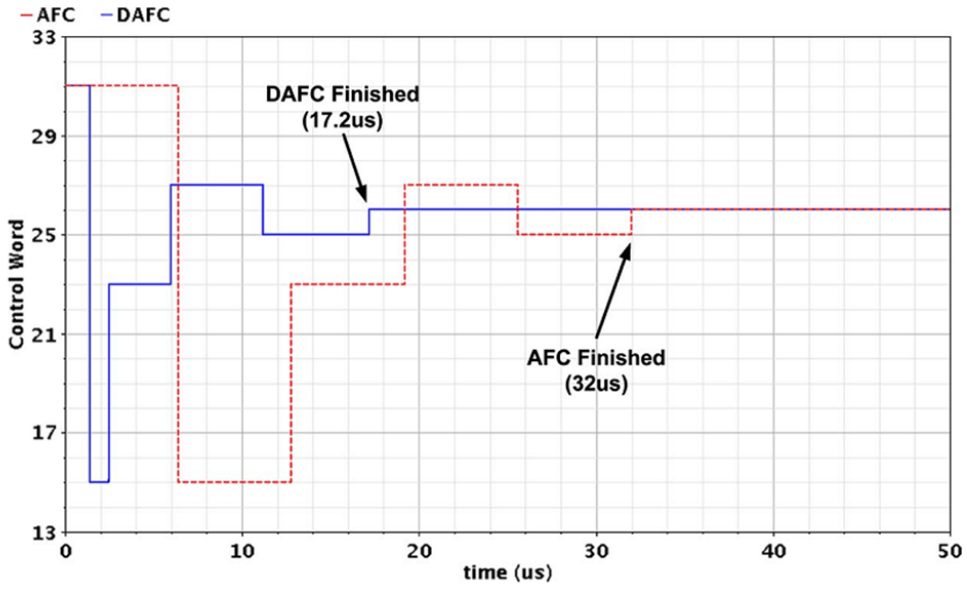

Figure 37: AFC versus DAFC simulation results

11.2.4 Multimodulus Divider and Band-Selecting Divider

Figure 38(a) shows the architecture of the multimodulus divider, which is formed by a chain of 2/3 divider cells. The first two bits of this divider are constructed by the source coupled logic (SCL) configuration, since SCL is more suitable for high-frequency operation. To save power and area, the remaining bits of the MMD are formed by CMOS logic, and an SCL-to-CMOS converter is inserted to convert these two logic levels. A modulus extension circuit is also included for the last two stages to increase the modulus range. Thus, the division ratio of the MMD is from 32 to 255. A well-known problem of this MMD is that the jitter introduced in every 2/3 divider cell accumulates, and hence, the output phase noise grows with the number of the divider cells used. A simple way to resolve this problem is to put a retiming flip-flop that is clocked by VCO at the output of the MMD.

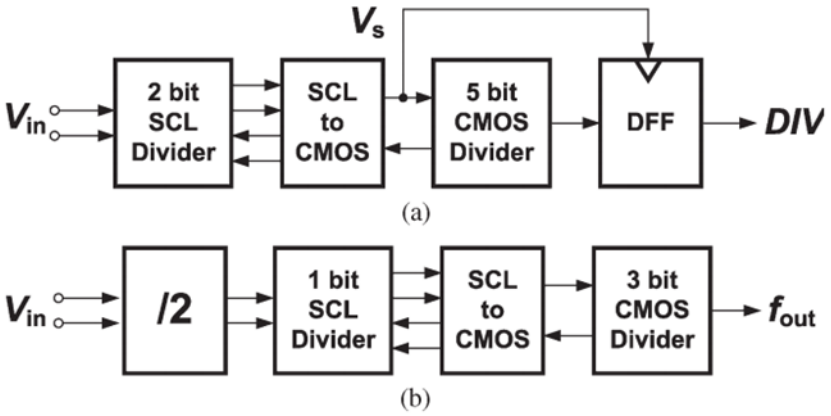

Figure 38: Multimodulus Divider Architecture

However, there are two drawbacks to do so: 1) The retiming flip-flop needs to operate at VCO frequency so that an SCL D flip-flop (DFF) and an extra SCL-to-CMOS converter are required, which increases lots of power consumption; and 2) the delay and jitter accumulated in the 2/3 divider cell chain may cause the metastability or cycle slip for high-frequency operation. This phenomenon is illustrated in Figure 39, where we take a simple divide-by-eight circuit as an example.

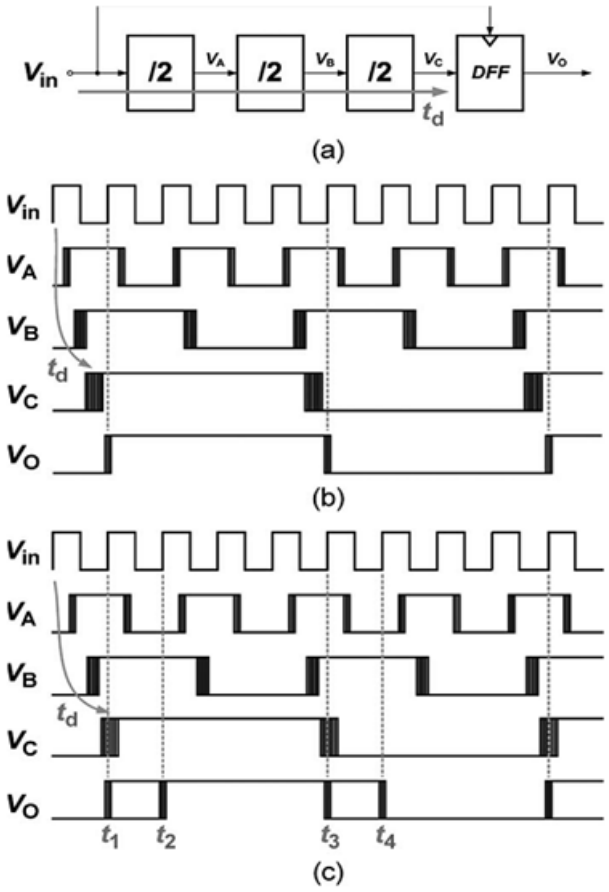

Figure 39: Metastability (a) A divide-by-eight circuit with retiming DFF. (b) Divider operation with small t_d. (c) Divider operation with large t_d

In Figure 39(a), three divide-by-two circuits are cascaded, and a DFF is used to retime the output signal. The time delay from the input Vin to the output of the third divide-by-two

cell VC is denoted by td. (Here, we ignore the path delay from Vin to DFF and the time delay in DFF for simplicity.) In Figure 39(b),td is short, and the jitter is small so that the retiming DFF can correctly sample the output value, whereas in Figure 39(c), if td becomes as long as one period of the input signal, the accumulated jitter causes uncertainty when the DFF samples VC and, thus, the rising and falling edge of the output signal VO may drift with time (VO may rise at t1or t2 and fall at t3 or t4). This uncertainty results in a variation of the output period and raises the phase noise at the output of the divider. Therefore, to avoid this phenomenon, the designer needs to carefully control the total delay in divider chain. The best choice of the delay length is to enter the output edge at the falling edge of the input signal. However, this is not that easy to be realized in all process, supply voltage, and temperature conditions, particularly when the input frequency is high. Therefore, a retiming method was proposed to fix this problem, which makes use of the VCO as well as the output signal at every stage to retime the MMD output. However, the DFF needs to operate at VCO frequency, the first drawback still exists. A compromising solution to these problems is to use a signal with a lower frequency to retime the output MMD, as shown in Figure 38(a), where the output signal of the SCL-to-CMOS converter VS is utilized as the retiming clock. Since VS has a much longer period than the time delay and jitter in the CMOS divider chain, metastability will not happen in this structure. On the other hand, the fact that VS is a CMOS logic signal means that the retiming DFF can be realized with CMOS logic circuit and thus, the power consumption and the area are reduced. However, the tradeoff is that the jitter accumulated in the first two 2/3 divider cells cannot be removed. Nevertheless, this is not a critical issue, because even with this additional jitter, the phase noise contributed by the MMD is still not the dominated source of the in-band phase noise. The band-selecting divider is depicted in Figure 38(b). The structure is the same as that of the MMD. The only difference is that the first 2/3 divider cell in the MMD is replaced by a divide by-two circuit, because the moduli required in this divider are all even numbers. The same modulus extension method is also employed in the three CMOS divider cells; hence, the modulus can range from 4 to 62.

11.2.5 $\triangle - \Sigma$ Modulator

The 24-bit MASH-111$\triangle - \Sigma$modulator shown in Figure 40 is chosen in this work for its unconditional stability and simplicity. The DSM consists of three accumulators, adders, and a quantization noise cancellation circuit, which is a combination of delay cells. The detail of the quantization noise cancellation circuit.

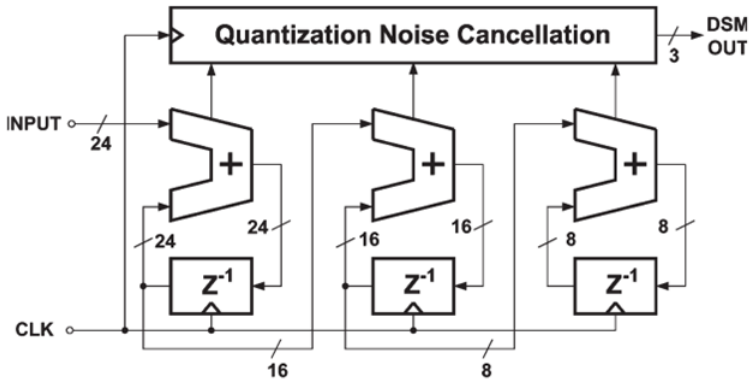

Figure 40: Block diagram of the DSM

The register lengths of the second and third accumulators are truncated to reduce the hardware as well as the power consumption. The frequency resolution depends on the bit

number of the DSM. The synthesized output frequency f_{OUT} can be written as:

$$f_{\mathrm{OUT}} = \frac{1}{M} f_{\mathrm{REF}} \left(N + \frac{K}{2^{24}} \right)$$

Where N is the integer division ratio, K is the input control word of the DSM, f_{REF} is the reference frequency, and M denotes the division ratio of the band-selecting divider. With a reference frequency of 40 MHz and M larger than four, the frequency resolution is smaller than 1 Hz. Therefore, the discrete frequency property of the DSM does not have any restriction to the behavior of the system since the resolution is by far smaller than the required frequency error 62.5 kHz.

11.2.6 PFD, CP, and LPF

The PFD employed in this frequency synthesizer is a typical tri state structure, which consists of two DFFs, an AND gate, and a delay cell to get rid of the dead zone. Figure 41 also illustrates the operation of the PFD. Signal DIV is the output of the MMD and REF is the reference clock, both of which serve as clocks of the flip-flops. If DIV comes earlier than REF, UP rises to make the CP charges the LPF so as to slow down the VCO. The charging period is proportional to the phase/frequency difference of REF and DIV so that the PFD, CP, and LPF can convert the phase/frequency errors into voltage signals.

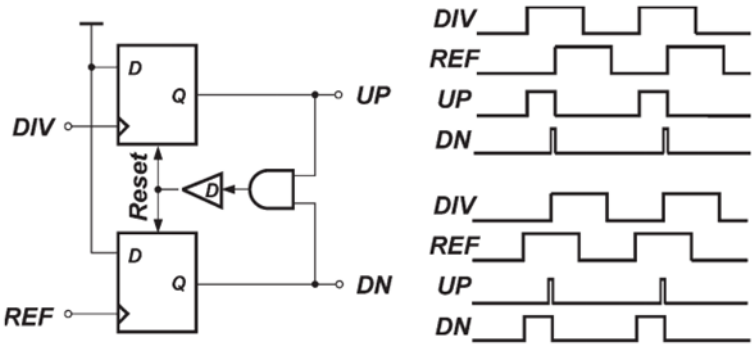

Figure 41: PFD operation

Figure 42 depicts the schematic of the charge pump with current steering switches and an active amplifier. Different from conventional single-ended charge pumps, current sources (M1,M2) in current steering charge pumps are never turned off, the output current is switched to another branch when the control signal is logic low. For example, if M3 is turned on to discharge the output voltage, M4 and M5 are turned off while M6 is on. The charging current from M2 flows through M6 and then sunk by the active amplifier. Since the current source M2 is never turned off, the drain voltage VP need not be discharged or charged when the UP current is switched between M4 and M6 so that the switching time can be improved. The unit gain amplifier is used to continuously track the output voltage and set the voltage at the drain of M1 and M2 to output voltage. Hence, the charge sharing effect can be alleviated when the switches are turned on.

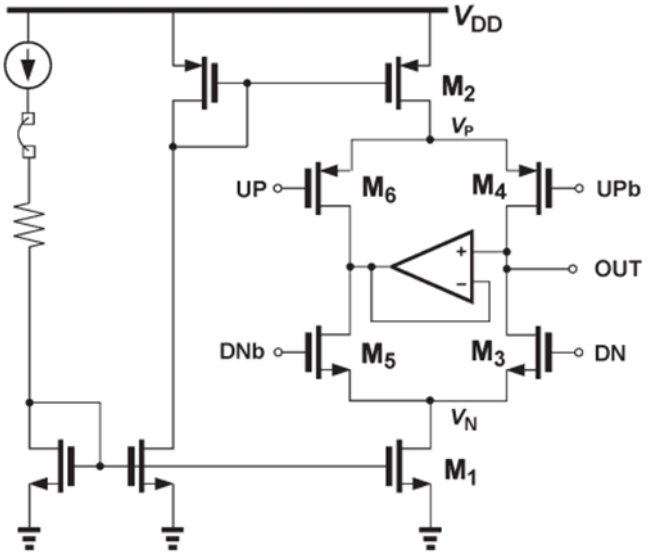

Figure 42: Charge Pump with current steering switches

The LPF used in this synthesizer is shown in Figure 43. It is a third-order off-chip passive resistance–capacitance filter, as shown. The LPF may also be integrated on-chip by using the capacitance multiplication method or the dual-path technique. However, in this work, the LPF is left off-chip; thus, we may optimize the loop bandwidth after measuring the phase noise. The resulting bandwidth is set to be 50 kHz to have an optimal performance of phase noise.

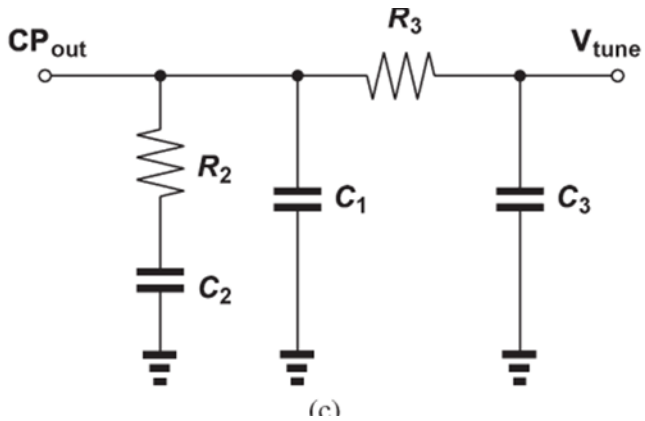

Figure 43: Third order LPF

11.3 Implemented VCO design : A Single-VCO (1.833 GHz - 4.31GHz)

11.3.1 VCO Rrchitecture

The implemented VCO architecture is the same shown in Figure 34. Figure 44 shows the circuit snapshot.

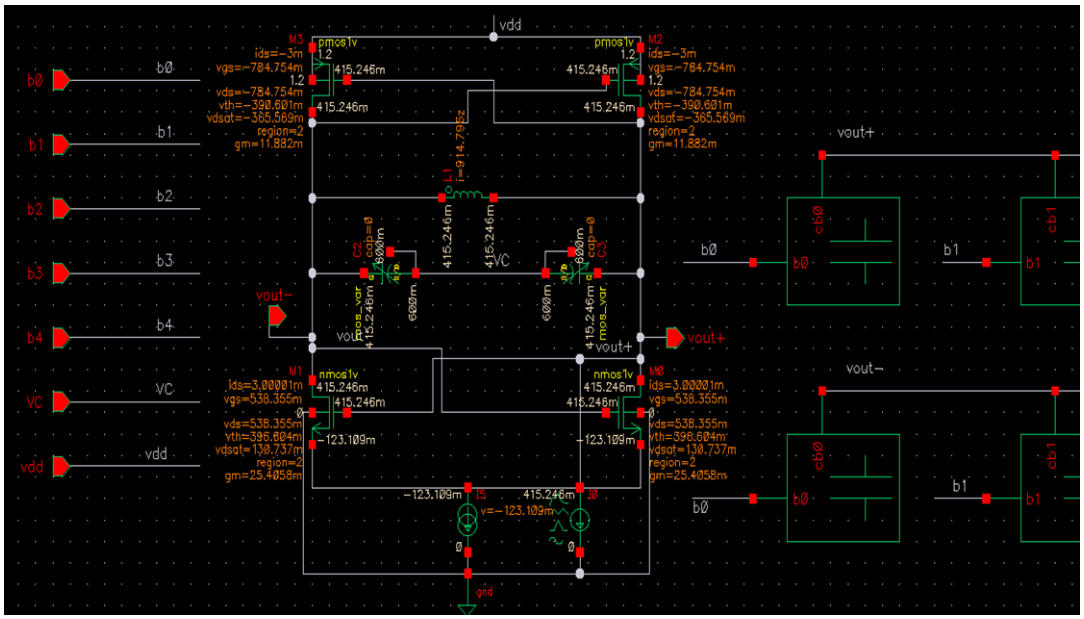

Figure 44: VCO schematic snapshot

11.3.2 A Procedure for the Design of LC VCOs

- Based on the power budget, determine the required tail current I_{ss}.
- Selecting the smallest inductor value that yields a parallel resistance of R_p at w_o. i.e., find the inductor with the maximum $Q = \frac{R_p}{Lw_o}$. This, of course, relies on detailed modeling and characterization of inductors in the technology at hand. Denote the capacitance contributed by the inductors to each node by C_p.
- Determining the dimensions of M1 and M2 such that they experience nearly complete switching with the given voltage swings. To minimize their capacitance contributions, choose minimum channel length for the transistors.
- Noting that the transistor, inductor, and load capacitances amount to a total of $C_{GS} + 4C_{GD} + C_{DB} + C_p + C_L$ at each output node, calculate the minimum varactor capacitance, Cvar,min , that can be added to reach the upper end of the tuning range.

$$w_{max} = \frac{1}{\sqrt{L * (C_{GS} + 4C_{GD} + C_{DB} + C_p + C_L + C_{var,min})}}$$

- Using proper varactor models, determine the maximum capacitance of such a varactor, Cvar,max. and compute the lower end of the tuning range.

$$w_{max} = \frac{1}{\sqrt{L * (C_{GS} + 4C_{GD} + C_{DB} + C_p + C_L + C_{var,mAX})}}$$

- The previous procedure is repeated many times to meet the specifications.
- The phase noise design equation:

$$S(\Delta\omega) = \frac{\pi^2}{2}\frac{kT}{I_{SS}^2}\left[\frac{3}{8}g_m + \frac{2}{R_p}\right]\frac{\omega_0^2}{4Q^2\Delta\omega^2}$$

It is shown that we have to increase the I_{ss} and gm to reduce phase noise.

11.3.3 Transient Analysis

Transient output waveform when b4b3b2b1b0 =“10000” , VC = 600mv is shown in Figure 45.

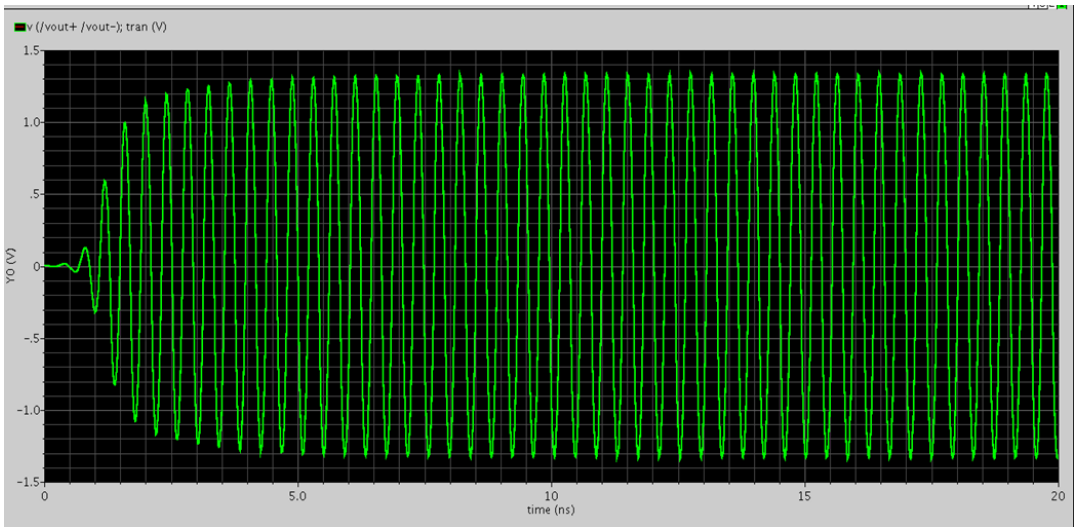

Figure 45: VCO output

Steady state output waveform when b4b3b2b1b0=“10000”, VC = 600mv is shown in Figure 46.

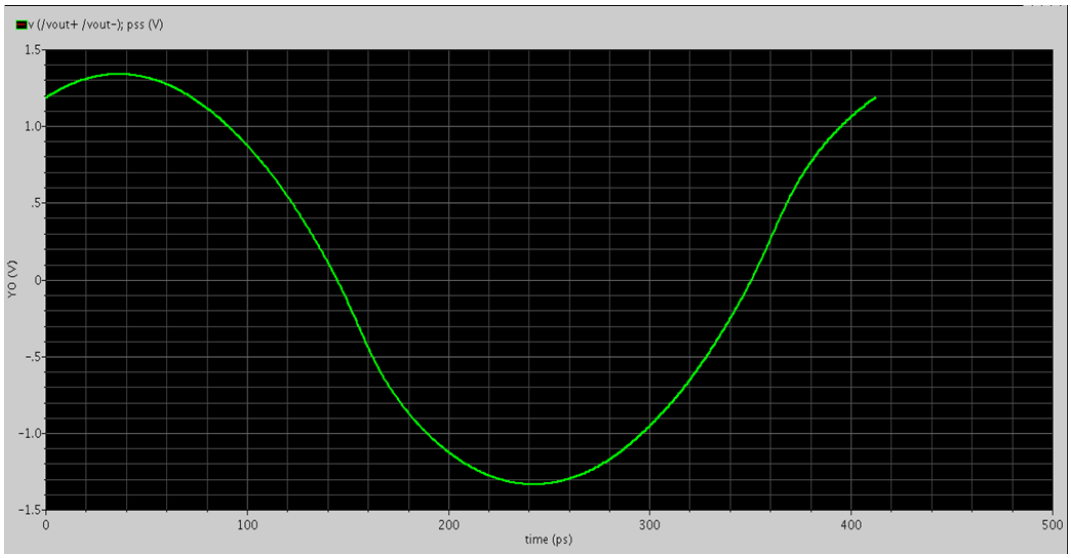

Figure 46: VCO Steady state output using PSS analysis

Output spectrum when b4b3b2b1b0 =“10000”, Vc=600mv is shown in Figure 47.

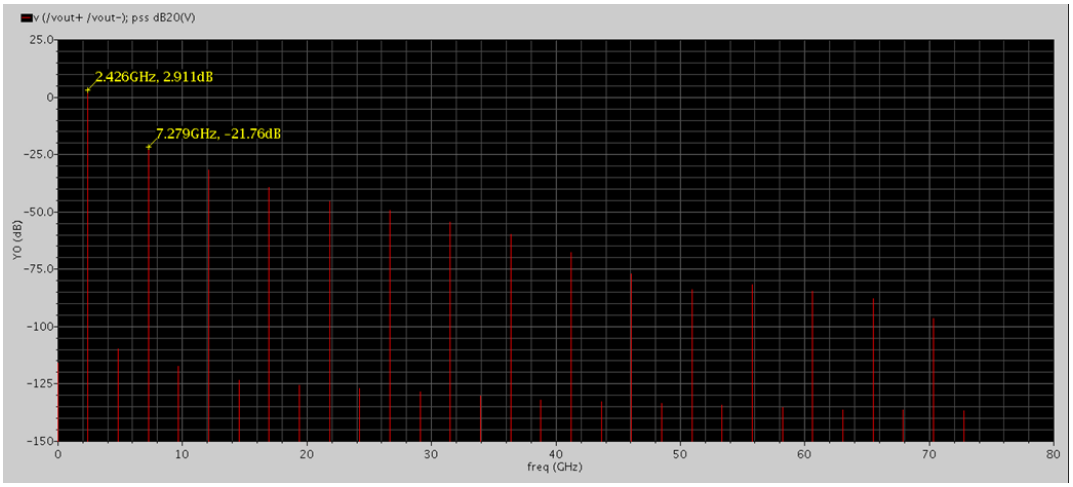

Figure 47: VCO ouptut frequency spectrum

Phase noise when b4b3b2b1b0 =“10000”, Vc=600mv is shown in Figure 48.

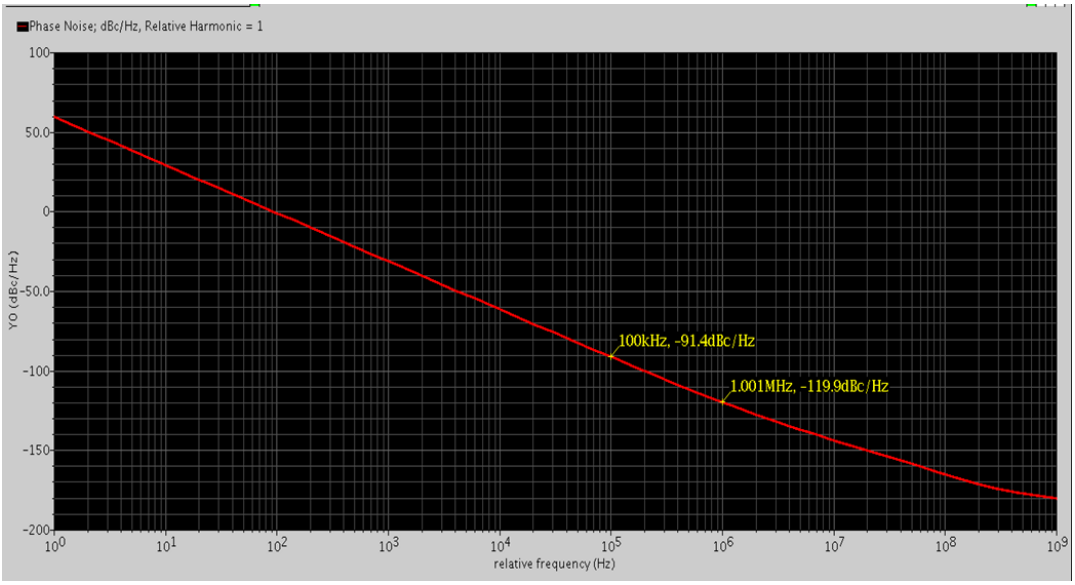

Figure 48: VCO phase noise

Tuning Curves is shown in Figure 49. As the control voltage (vc) changes, the outpur VCO steady state frequency changes. Each curve represents a code setting.

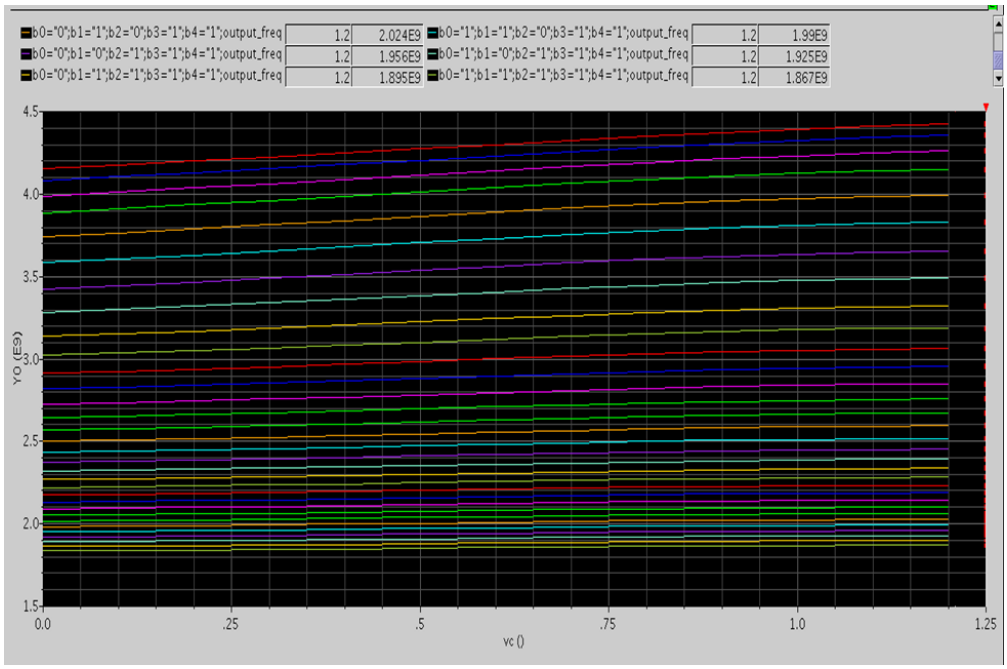

Figure 49: VCO tuning curve

Design parameters are listed in Table 18.

Table 19: VCO design parameters

Parameter	**value**
W/L of NMOS and PMOS	50µ/130n
W/L of the unit cell switching NMOS of the Cap-bank	4µ/130n
Total W/L of switching NMOSs of the Cap-bank	248µ/130n
Unit capacitance of the cap-bank	150 fF
C_{max} of the varactor @ VC=0 V	211.779 fF
C_{min} of the varactor @ VC = 1.2V	83.707 fF
Current draws from a 1.2-V supply	6 mA
Total Power	7.2 mW

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Part IV
Variable-Gain Amplifier

13 INTRODUCTION

VGA is one of the most essential building blocks for low voltage applications such as wireless communication and mobile imaging applications. Variable gain amplifier (VGA) is signal-conditioning amplifiers with electronically settable voltage gain. There are analog VGAs and digital VGAs, or DVGAs. An analog voltage controls the gain in both, which differ in how it is applied. VGAs are available from dc to gigahertz frequencies and in a variety of I/O configurations. Variable gain amplifiers (VGAs) have been used in a variety of remote sensing and communications equipment for more than a half-century. Applications ranging from ultra-sound, radar, wireless communications and even speech analysis have utilized variable gain in an attempt to enhance dynamic performance.

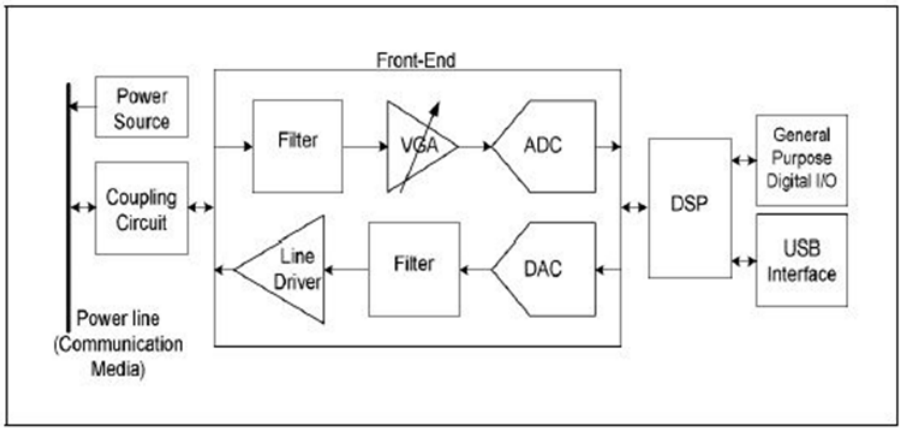

Figure 50: Typical Wireline transceiver

In communication receivers, VGA is typically employed in a feedback loop to realize an automatic gain control (AGC), to provide constant signal power to baseband analog-to-digital converter (ADC) for unpredictable received signal strengths. At present, a key design aspect for VGA is the low power dissipation, wide bandwidth and low cost.

VGA, as well as other circuits, are required to operate with low power supply voltage and low power consumption. As the process technologies develop, the maximum allowable supply voltage will scale down. It is inevitable that most low power integrated circuits will have to operate with power supply voltages between 1 V to 1.5 V. It is very challenging to design a VGA with high linearity and wide bandwidth with low supply voltage and low power consumption. In addition, VGA is generally required to maintain high linearity and low noise over the entire bandwidth and gain range. It is also important that the bandwidth of the amplifier remains constant when the voltage gain is varied and this can be obtained by employing current-mode techniques.

14 VGA FUNDAMENTALS

The design of an amplifier requires a detailed analysis of the trade-offs involved in meeting the specifications. For instance, the higher the gain of the amplifier, the lower its bandwidth and the higher its non-linearity. Hence, selection of a particular topology is based upon the

feasibility of the design meeting most of the specifications, as well as a careful consideration of the compromises that need to be made for certain parameters while ensuring that the system still works as expected.

14.1 Gain and Bandwidth Specifications

As we can say there's trade-off between the bandwidth of the amplifier and the gain of the amplifier as when the gain is higher the bandwidth will be limited so we should choose our design carefully.

Different techniques to enhance the gain and the bandwidth can be used as follows:

14.1.1 Gain Enhancement Techniques

1- Cascoding

The amplifier in Figure 51 has higher gain than the normal amplifier (diff. pair) gain was ≈ gm (ron // rop) while the folded cascode has gain ≈ $(gm\,ron)^2$

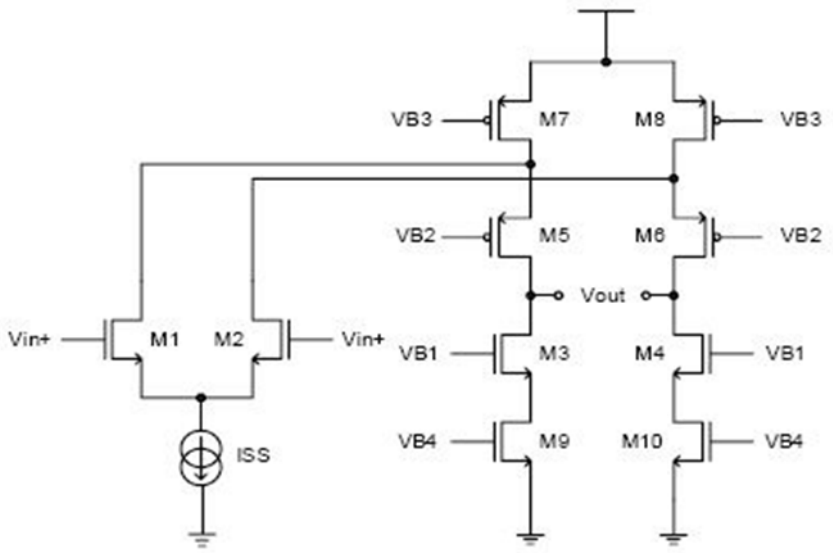

Figure 51: Folded Cascode Amplifier

2- Gain boosting

Gain boosting can be done by many ways one of these to use differential pair amplifiers with diode-connected loads, But the loads consume voltage headroom, limiting the output voltage swing, gain and the input common mode range. In order to obtain a higher gain, the transconductance (gm) of the load transistor has to be decreased. This can be done by decreasing the W/L value of the load. However, a disadvantage of this solution is the corresponding increase in the overdrive voltage, which in turn lowers the output common mode level as well as the voltage swing. This problem can be avoided by adding PMOS current sources in parallel to the load transistors, as indicated in Figure 52. Since the current is now split between the load and the current source, the W/L value of the load transistor can be decreased without changing the overdrive voltage. Hence, the transconductance of the load can be decreased without compromising the output voltage swing.

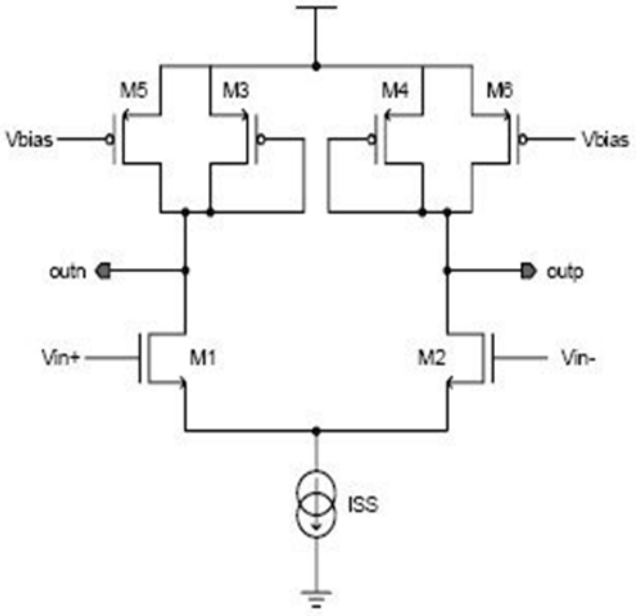

Figure 52: Addition of current sources to increase the gain of differential amplifier with diode connected load

If transistors M5 and M6 of Figure 52 carry 40% of the drain current of M1 and M2, and the load transistors M3 and M4 carry the remaining 60%, their transconductance decreases by a factor of 2/5 since the W/L ratios of M3 and M4 can also be decreased by the same amount without affecting their overdrive voltage. Thus, the differential gain increases by approximately 5/2 times that of the gain when the PMOS current sources are not included in the circuit. A disadvantage of this method of increasing the gain is that the current sources add parasitic capacitances to the output node of the circuit, slightly lowering the -3dB bandwidth.

14.1.2 Bandwidth enhancement techniques:

1- Capacitive neutralization to increase bandwidth

This technique (as shown in Figure 53) is sometimes used in wideband circuits to increase the bandwidth of multistage amplifiers.

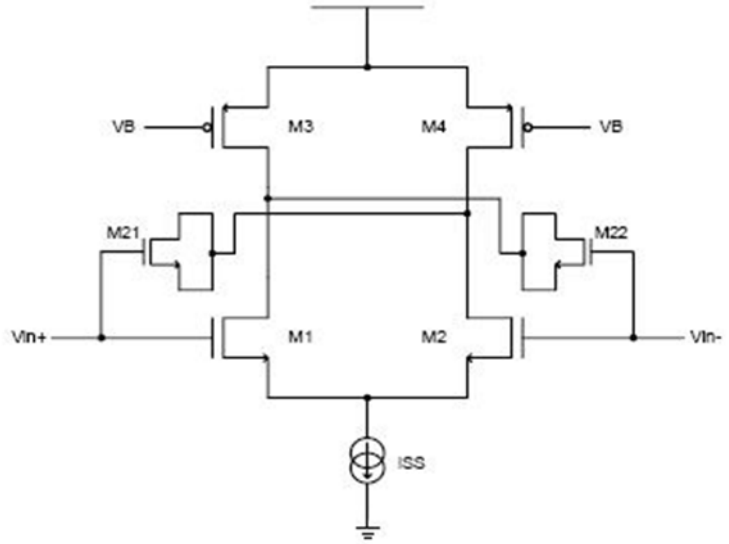

Figure 53: Capacitive neutralization with MOS transistors as capacitors

It can be proven that $C_{in} = C_{GS1} + C_{GD1}(1 - A_v) + C_{21}(1 - A_v)$. If the value of C_{21} is selected such that $C_{21} = C_{GD1}$ then the equation will be simplified to: $C_{in} = C_{GS1} + 2C_{GD1}$ This is very similar to the input capacitance of a cascode configuration. While the disadvantage of the capacitive neutralization technique is that the junction capacitances of transistors M21 and M22 in Figure 53 load the nodes to which their drains are connected. This results in a lowering of the pole associated with that node.

2- Inductive Peaking

Active inductive peaking is one of the methods employed to increase the bandwidth of circuits used in wideband applications. The structure used is shown in Figure 54, and comprises of a PMOS transistor (which acts as the load for the main amplifier), an NMOS transistor with its gate and source connected to the drain and gate respectively of the load as shown, a capacitor and a current source.

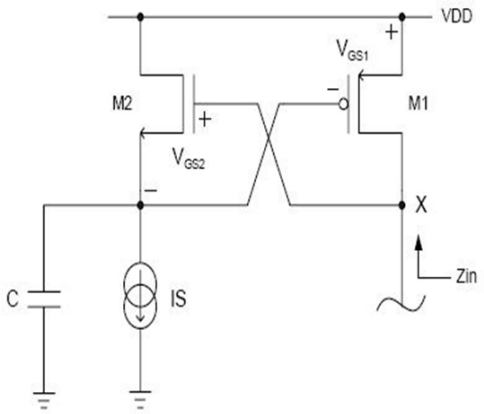

Figure 54: Active inductive peaking

It can be proven that $Zin = \frac{C}{gm1gm2}(s + \frac{gm2}{C})$. The expression for Zin indicates that the low frequency input impedance of the structure is approximately 1/gm1 but a zero is introduced at

a frequency gm2/C, giving rise to high frequency peaking in the gain of the VGA in which this structure is used as an active load. At high frequencies, the inductance forms a parallel resonant circuit with the parasitic capacitances associated with the drain of the PMOS transistor. The -3dB bandwidth of the VGA can be extended by properly adjusting the value of the capacitance C and the transconductance of transistor M1. Hence, when this structure is used as the load of the VGA, the DC output voltage is ideally well defined.

14.2 Noise and Linearity

There is trade-off between the noise and the linearity of the VGA as when we increase the gain of the amplifier the input referred noise is reduced while the linearity of the amplifier is reduced (gain 1-dB compression and IIP3) and if the gain is reduced the linearity of the amplifier is improved while the input referred noise increases so we should choose our architecture carefully .

14.3 Power Consumption and Output Swing

We need to reduce the power consumption of the VGA as much as possible but it depends on the application , the gain range and the noise .

while we need to achieve desired output swing to be suitable for the full scale voltage of the ADC .

15 VGA ARCHITECTURES REVIEW

This section covers various existing digitally controlled and analog controlled VGA structures. The gain control scheme and the linearization technique are discussed, and their advantages and disadvantages are compared between different structures.

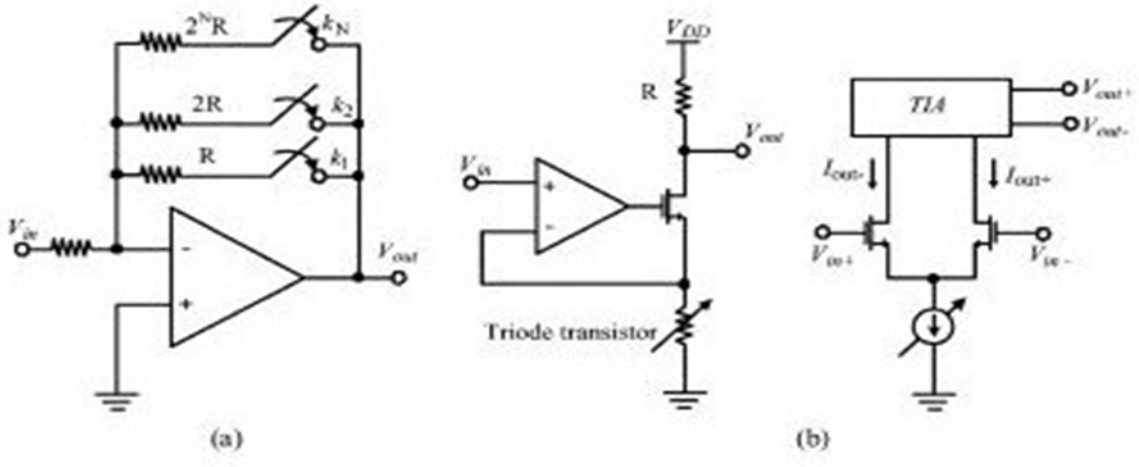

Figure 55: (a) Digitally controlled VGA (b) Analog controlled VGA

15.1 Digitally Controlled VGA Structures

15.1.1 Non-Inverting Amplifier

In this case we can select different gain levels by using different digital codes.

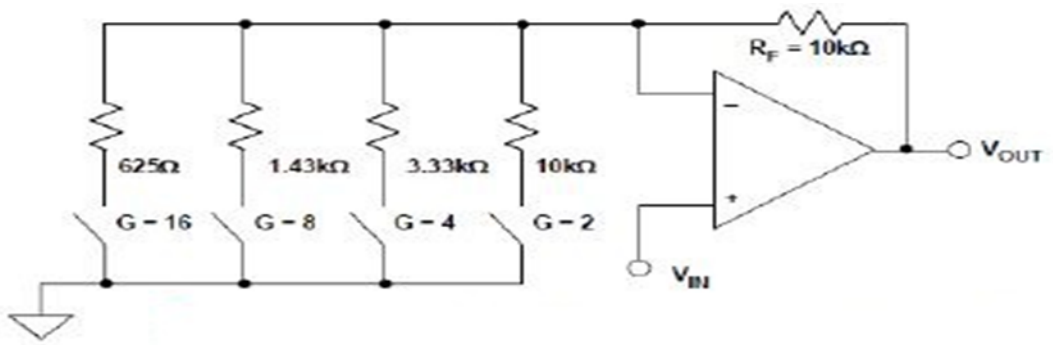

Figure 56: Non-inverting amplifier

Since the gain is given by $G = 1 + \frac{R_2}{R_1}$, We select desired gain by activating the corresponding switch.

Design Considerations:

- This design can't work as attenuator use alternative architecture (inverting amp.)
- We need to make the switch resistance much less than the resistors to get precise gain values.
- Carefully size switches as it affects the linearity of the circuit.
- To minimize the input referred noise use small values of resistances as much as possible (trade of with linearity)

15.1.2 Alternative Design of Non-Inverting Amplifier

Alternate architecture makes the gain insensitive to the switch resistance RON as there is no current flow in the switch so we removed the effect of the switch non-linearity.

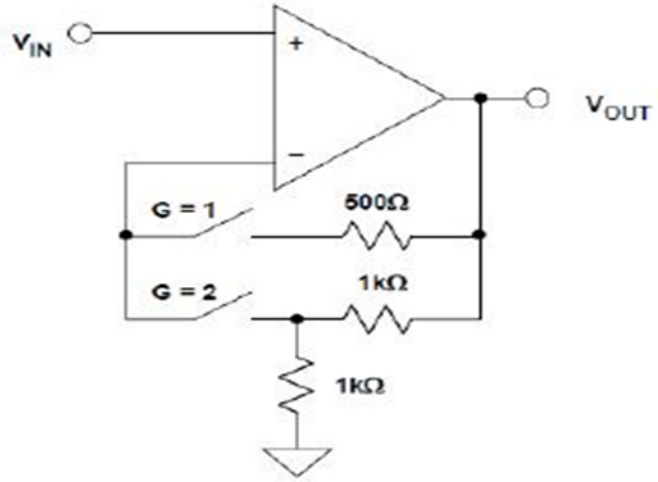

Figure 57: Alternative design of non-inverting amplifier

15.2 Analog Controlled VGA Structures

15.2.1 Inverting Amplifier

The gain value can be changed by changing the control voltages applied to the analog switches which operate in triode that will change their on resistance resulting in changing the gain value . A higher gain range can be achieved by sweeping the control voltages in opposite way to get max and min values of the gain. $G = -\frac{R_2}{R_1}$.

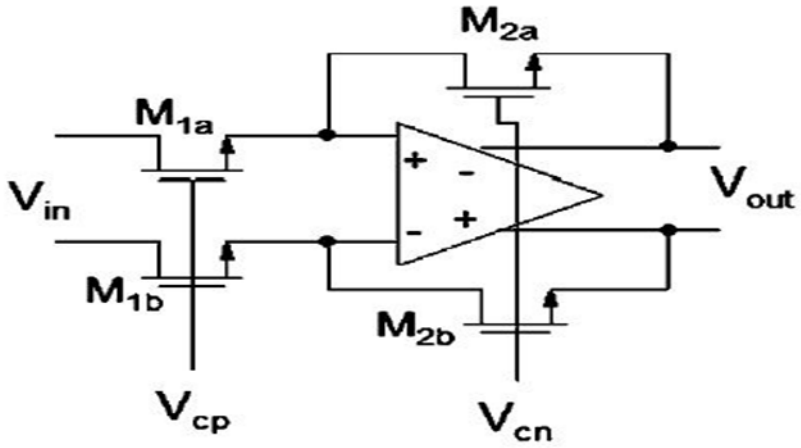

Figure 58: Inverting amp. with analog switches

The disadvantage of this circuit that the that the switch is in the signal path and the on resistance of the switch changes with the input voltage so we better use linear switches than single switch by using transmission gates.

15.2.2 Differential Pair with Diode-connected Load

The gain of the amplifier shown in Figure 59 can be controlled by changing the values of the transconductance of the transistors M1 M2 M3 M4 and this can be achieved by changing the value of the current flow in each of them such that the net current in both of them is equal to the current flow in the PMOS current source. The gain is given by:

$$A_v = \frac{g_{m1}}{g_{m3}} = \sqrt{\frac{\mu_n (W/L)_1}{\mu_p (W/L)_3}}$$

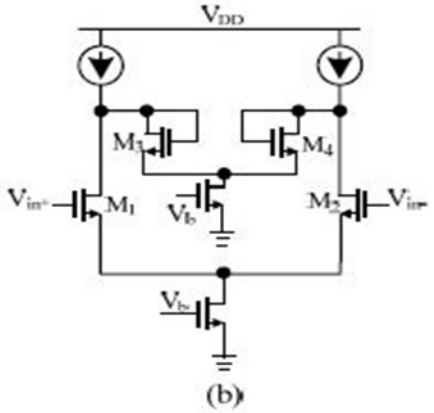

Figure 59: Differential pair with diode connected load

This trnasconductance cell can be used as a building unit of a full VGA architecture. As shown in Figures 60, 61 the gain is controlled by changing the value of C1 , C2 then the corresponding transconductance will be changed and also the gain of the circuit . the control circuit that generates the control signals C1 ,C2 is shown in Figure 62.

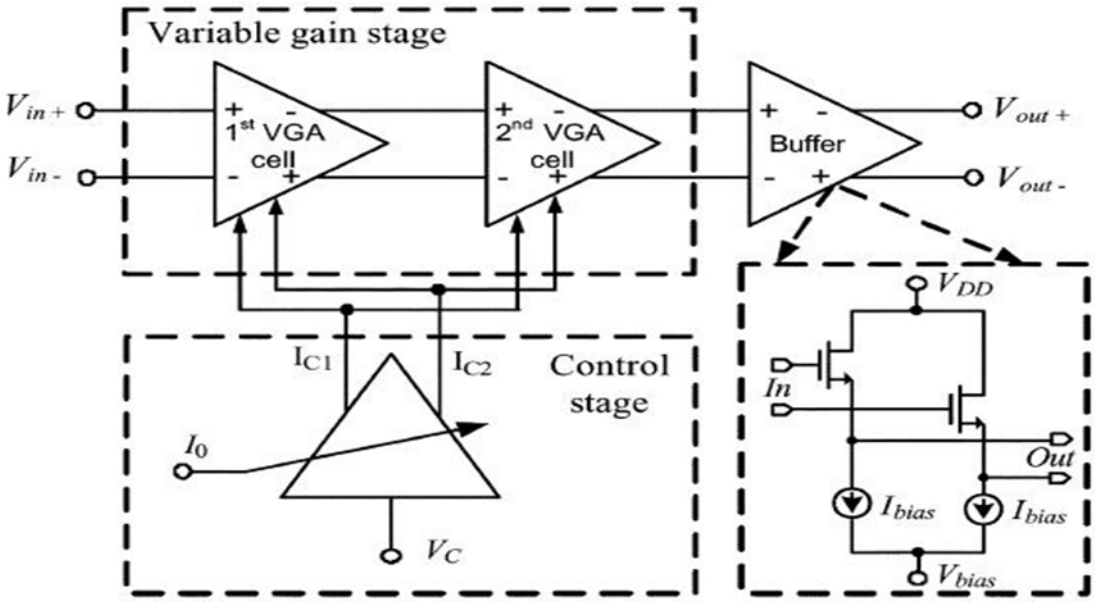

Figure 60: VGA block diagram

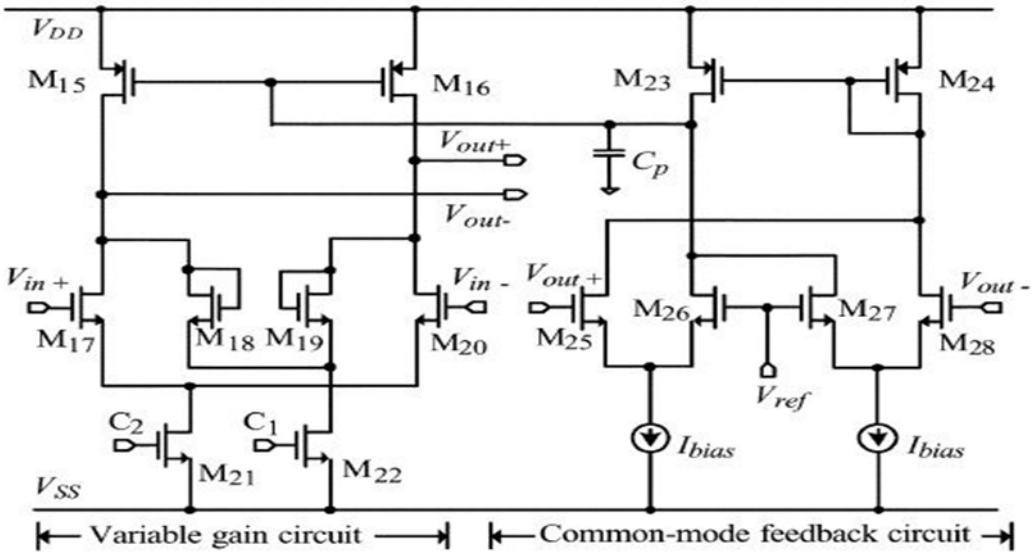

Figure 61: Full VGA design with CMFB

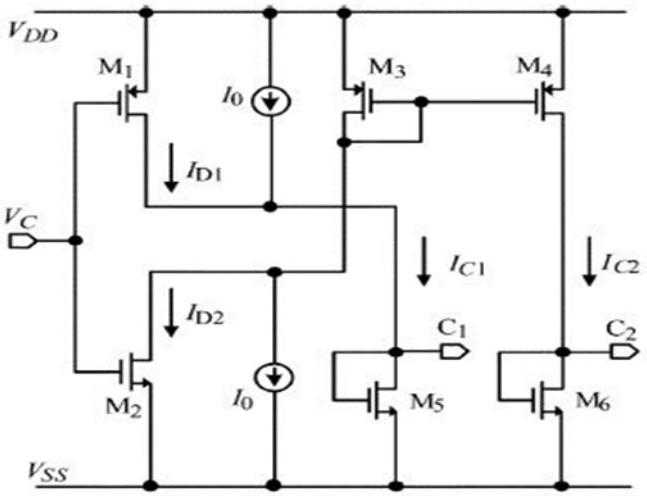

Figure 62: Schematic of the control stage

Changing the value of I_o will change the gain controls C1 ,C2 and we can control the current Io by the next reference current generator in Figure 63.

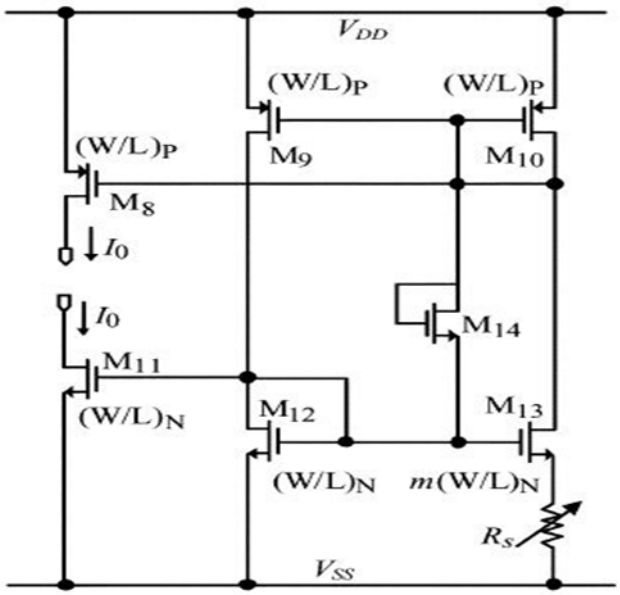

Figure 63: Circuit schematic of the current Io generator

15.2.3 Attenuator-Amplifier & Amplifier-Attenuator

Another way to make VGA is to use multi step attenuator followed by fixed gain stage or fixed gain stage followed by multi step attenuator as shown in Figure 64.

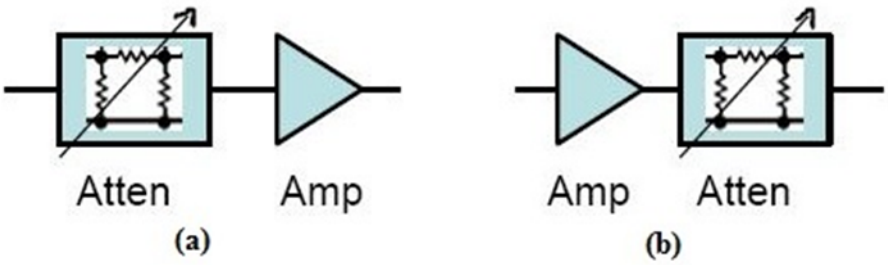

Figure 64: (a) Attenuator-Amplifier (b) Amplifier-Attenuator

The first case of the attenuator then the fixed gain is better if the linearity of the VGA is more important as this design has better linearity and worst input referred noise and the second design is better if we care more about the input referred noise more as the noise will be divided by fixed gain to be referred to the input.

15.2.4 VGA Based on Analog Multiplier & Current Mirror Amplifiers

The input voltage is sensed by OTA and then the output differential current is multiplied into many steps depend on the desired gain values and then the total current flow in the load resistance to achieve the desired gain value . The advantages of this architecture is that it has low headroom (high swing).

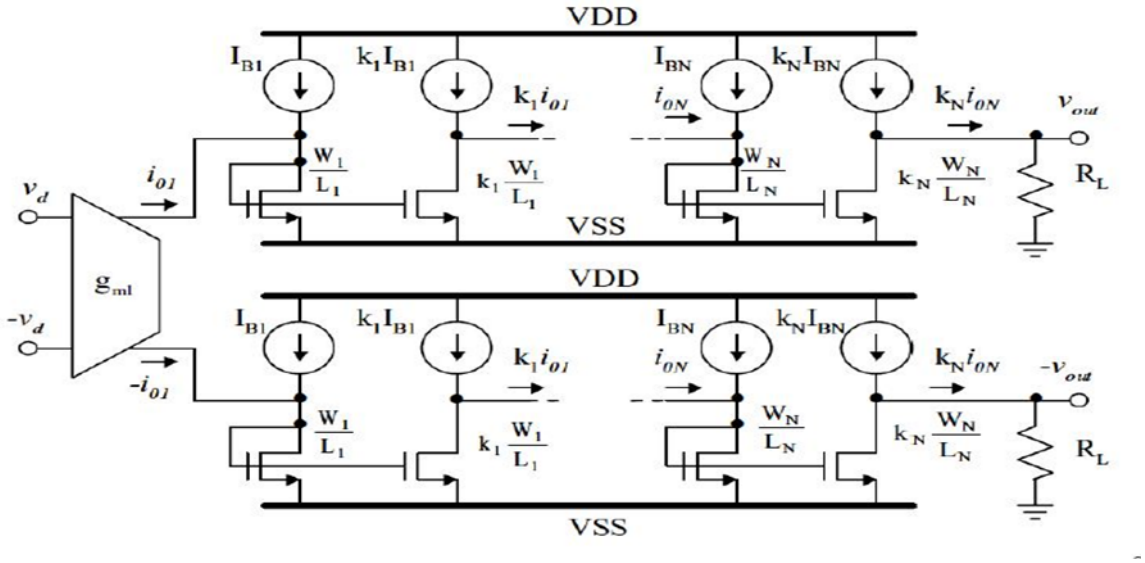

Figure 65: Analog Multiplier & Current Mirror Amplifiers VGA

15.2.5 Source Degeneration VGA

A circuit is said to be linear if the circuit is designed into that the gain is less dependent on the bias condition and the input level. A simple way to realize this principle is called source degeneration . A resistor is inserted at the source of the transistor in a common-source amplifier, as shown in Figure 66 . The source degeneration VGA is often used in open-loop system. The most common differential structure is shown in Figure 66.

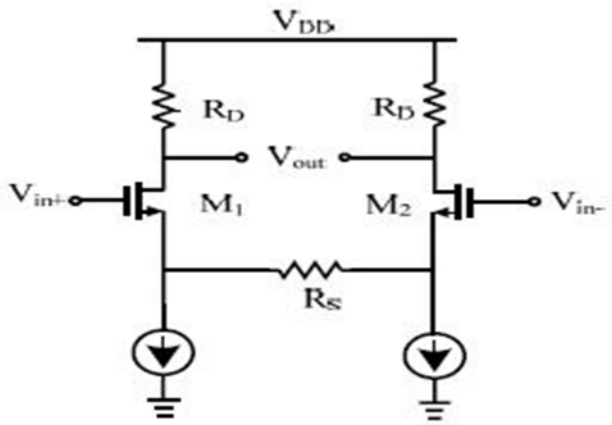

Figure 66: Differential pair with source degeneration

The basic idea is the same as that in the single-ended source degenerated the larger degeneration resistor is the highly linearity achieved at the expense of decreasing the transconductance of the amplifier, which essentially reduces the gain. The transconductance of the differential pair with source degeneration is determined by Gm = gm/(1+gm Rs /2) where Rs is the source degeneration resistor and gmRs/2 is the source degeneration factor. If the source degeneration factor is much larger than 1 the equation will be simplified to Gm = 2/Rs. Under this condition, the transconductance of this configuration is simply determined by the source degeneration resistor. By changing the value of Rs, the amplifier gain is tuned. However, the gain of the amplifier decreases dramatically, and the stage becomes noisier. A linear and accurate resistor is required to maintain the linearity and keep the gain accurate for this topology. Such a high

quality passive element sometimes is not available in the digital CMOS technology. A MOS transistor working in a deep-triode region functions as a resistor, and the resistance linearly depends on the bias voltage. Such a transistor can be used to replace the resistor . to increase the gain we will need to increase the load resistance and that will limit the output swing so we can use active loads and control the gain by the feedback resistors.

Design considerations:

To have linear relation for the gain independent of the input transconductance then we have to increase the value of Rs so that the gain depend on the values of Rl and Rs but when we increase Rs the gain range will be reduced as Rs increases so the other way is to increase the effective Gm of the input transistor then we can use smaller values for Rs and the gain range is larger . The Gm boosting technique is shown in Figure 67.

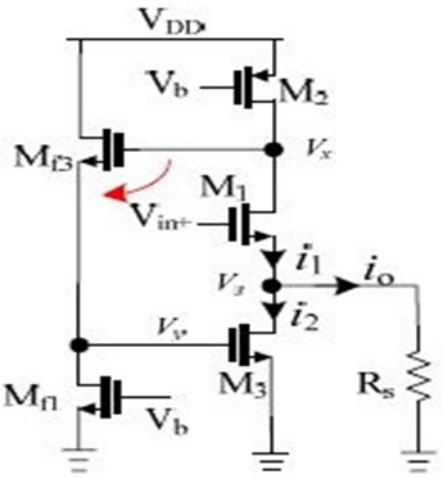

Figure 67: Gm Boosting technique

Figure 67 is the gm-boosted circuit, where a feedback loop is added into the source degeneration amplifier. The input voltage is first converted into a current flowing through M1, and part of the current is then converted back to voltage at the drain of M1 and M2. The signal voltage at the drain of M1 is shifted by Mf3, and then applied to the gate of M3, which converts the voltage signal into a current. The current is subtracted from the signal current in M1 at the source, and the left current flows to the resistor this current is quite linear current so it will be mirrored to another linear stage to achieve the desired gain value.

The transconductance of this source degeneration stage is boosted by a factor of $[1 + gm2(ro1||ro3)]$, which is a quite large value compare to the normal source degenerated stage . $Gm = [1 + gm2(ro1||r03)]gm1$ The full schematic of the VGA is shown in Figure 68.

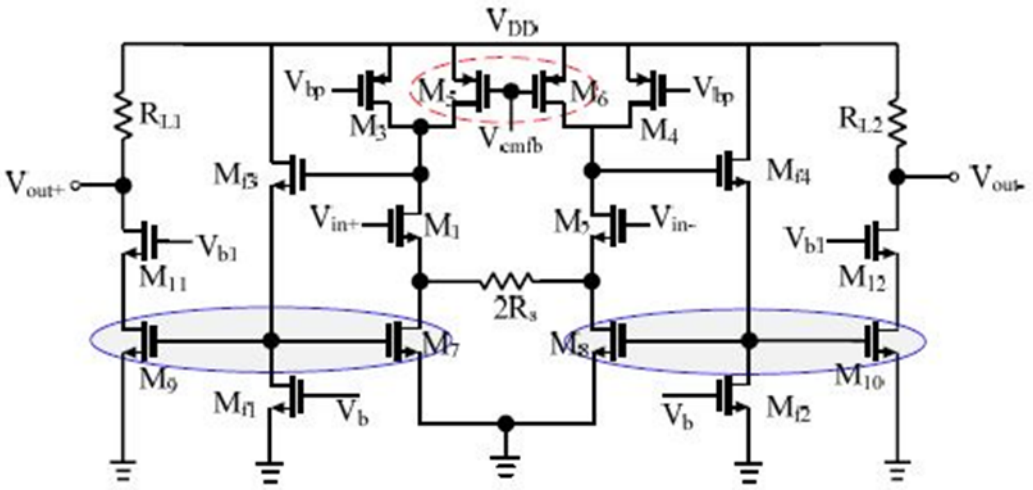

Figure 68: Full schematic of Gm boosted VGA

The overall gain of the two-stage Opamp can be easily derived to be $Av = N\frac{R_L}{R_S}$ While N is the current ratio between M7 , M9 and the gain can be controlled through this current ratio or through the two resistors and both are linear relations.

15.2.6 Cascade of a Linear Transconductance and a Tinear Transimpedance Amplifier

The input voltage signal is transferred into current with current gain Gm of the first stage and then this current is transferred into voltage after passing it to the transimpedance amplifier.

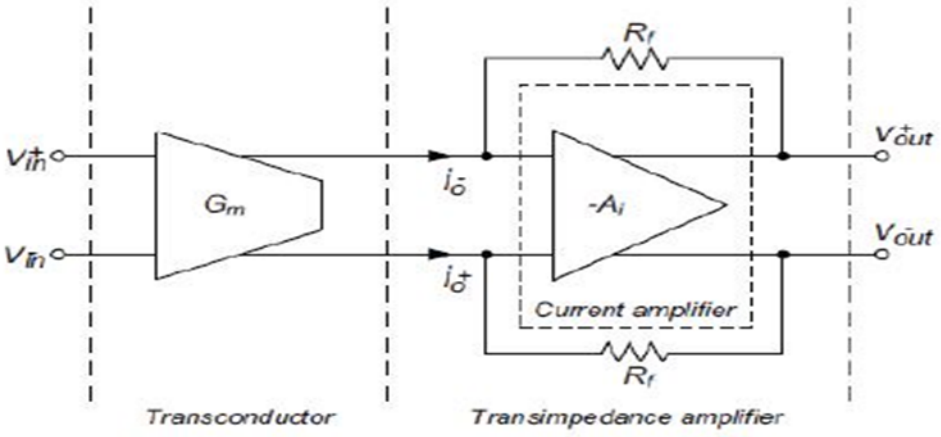

Figure 69: The Block diagram of the proposed VGA

This allows constant bandwidth when varying the voltage gain. The voltage gain of the VGA circuit is the product of the transconductance gain (Gm) and the transimpedance gain (Rm). The transimpedance gain is given by $R_m = -\frac{R_f A_i - R_{in}}{1+A_i}$. Where Rin and Ai, respectively, are the input resistance and the current gain of the current amplifier. Note that, when Ai >> 1, we have Rm ≈ –Rf. Then a linear Gm and a high gain for the op-amp is required to have linear gain. The circuit schematic is shown in Figure 70.

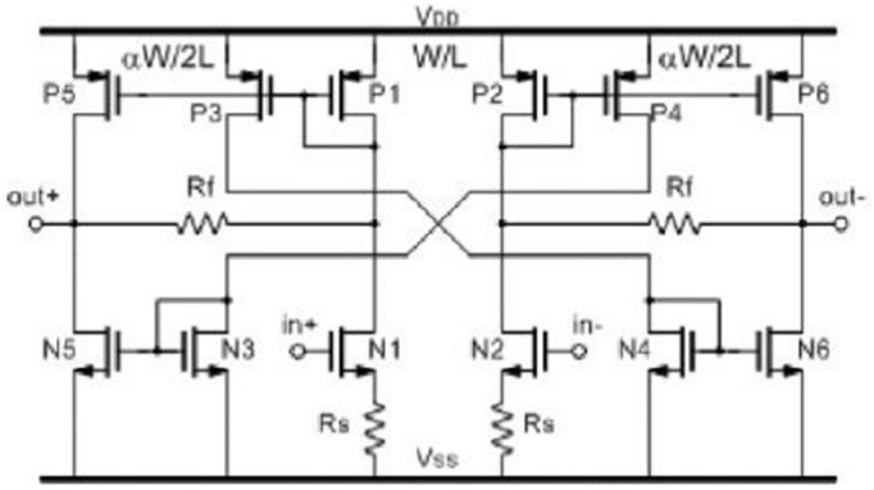

Figure 70: Gm – TIA VGA schematic

16 A 60 dB DIGITALLY PROGRAMMABLE GAIN AMPLIFIER

The input signal into the power line can be attenuated as large as 60 dB. To well amplify the input signal into a predefined level at the output of VGA, a 5 dB gain variation for each step is desired. The gain is controlled digitally by the control signals 32 coming from the flowing DSP system . The block diagram of the VGA is shown in the Figure 71.

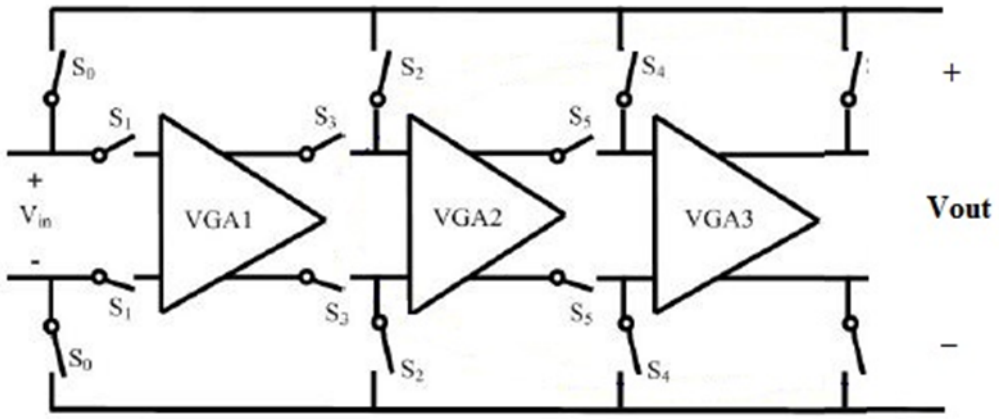

Figure 71: VGA Block diagram

We can select the number of operating stages to achieve the corresponding current as each stage has gain range almost 20 dB for each stage so for the low gains we better bypass the 2nd and the 3rd stages to reduce the power for low gain bur for high gain levels we will use the 3 stages to achieve this gain value.

Table 20: VGA Design Specifications

Parameter	value
Gain Range	-20 dB : 60 dB
Bandwidth	Up to 100 MHz
Noise	< 14 bit ADC quant noise < 8* 10^{-10} V^2 /Hz
Linearity	IIP3 > 10 dBm at 0 dB gain
Output swing	1.6v V_{p-p} differentially

16.1 The First Stage: Low Noise, High Gain Amplifier

As we discussed before the first stage should be optimized on noise performance. The linearity is not a challenge since this stage only receives small-signal. To optimize the noise performance, the thermal noise and flicker noise of the transistors in the stage itself is optimized. On the other hand, the gain is designed to be high to suppress the noise coming from the following cascaded stages. The first stage consists of 2 main stages the first is resistor attenuator to achieve the negative gain levels in dB followed by source degenerated amplifier with active load and CMFB resistors are used to achieve the desired gain level up to 15 dB. The block of the first stage VGA is shown in Figure 72.

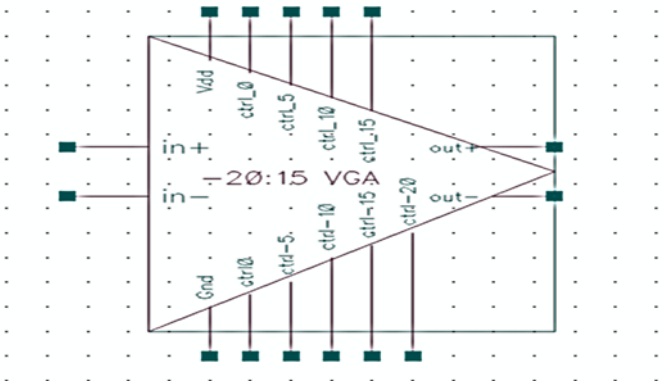

Figure 72: VGA symbol

As we can see we have 9 control signals required for this stage so we need 4 bit DAC to generate the corresponding control signals we can also use the same DAC for 2.5 dB steps . The first part of the VGA is resistor attenuator with gain step equal 5 dB as shown in Figure 73.

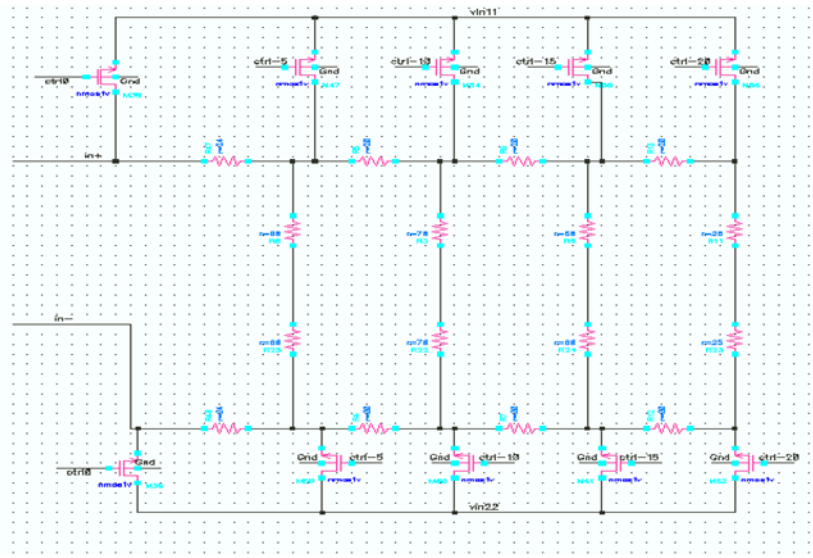

Figure 73: 24 resistor attenuator schematic

We select between the different gain levels through the NMOS switches the switch sizes are large to reduce the noise produced by it.

While the second stage is shown in figure 25 and the CMFB op-amp in Figure 74.

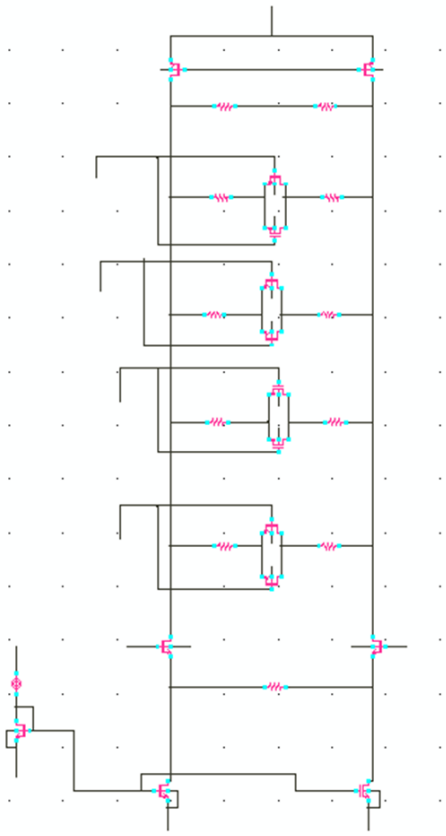

Figure 74: The main Core of VGA schematic

As we can see we have different gain levels controlled by the digital signals to select the proper gain level . here we can control the gain by changing the value of the load resistances increasing it to have higher gain level while using active loads with high load resistance so it doesn't affect the gain values .

The CMFB circuit (Figure 75) is used to define the bias voltage of the PMOS current sources as if any mismatch occurs it can handle it to set the output CM back to the same value.

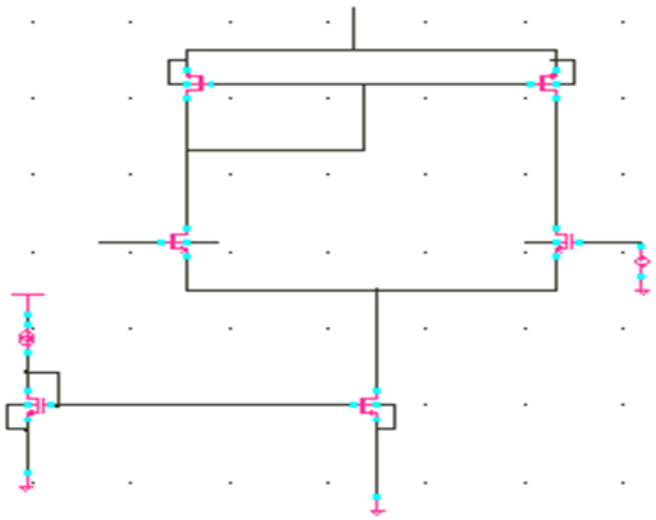

Figure 75: CMFB op-amp

16.2 Simulation Results

In this design we we used 0.18um CMOS technology m and we used the TSMC design kits . and the spectre simulator in cadence design environment have been utilized to perform the simulations .

Several analysis were done such as DC , AC , Transient , PSS , noise were used to check the performance of the circuit.

Simulation test bench

In Figure 76 we can see the simulation test bench for the first stage of the VGA . The test bench is used to check for the system response and performance to check linearity and frequency response and noise and bandwidth .

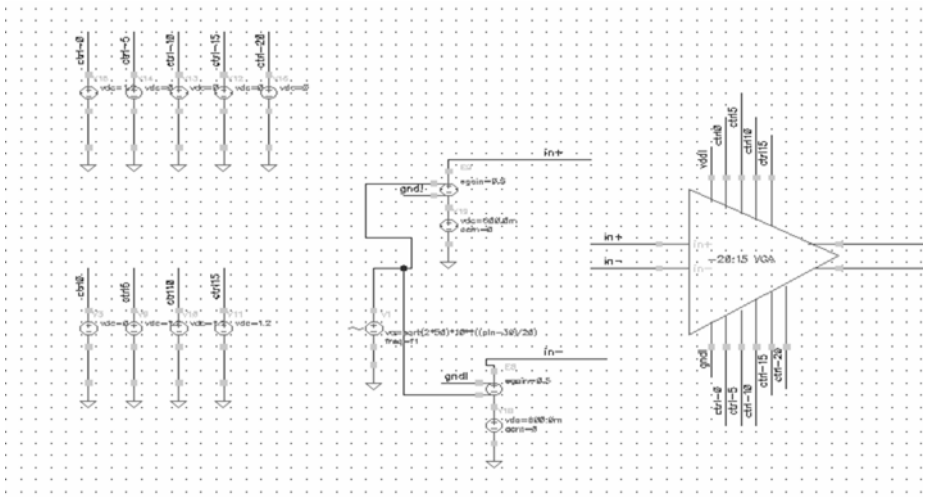

Figure 76: VGA test bench

Frequency Response

The simulated frequency response of the first stage VGA for all gain levels is shown in Figure 77.

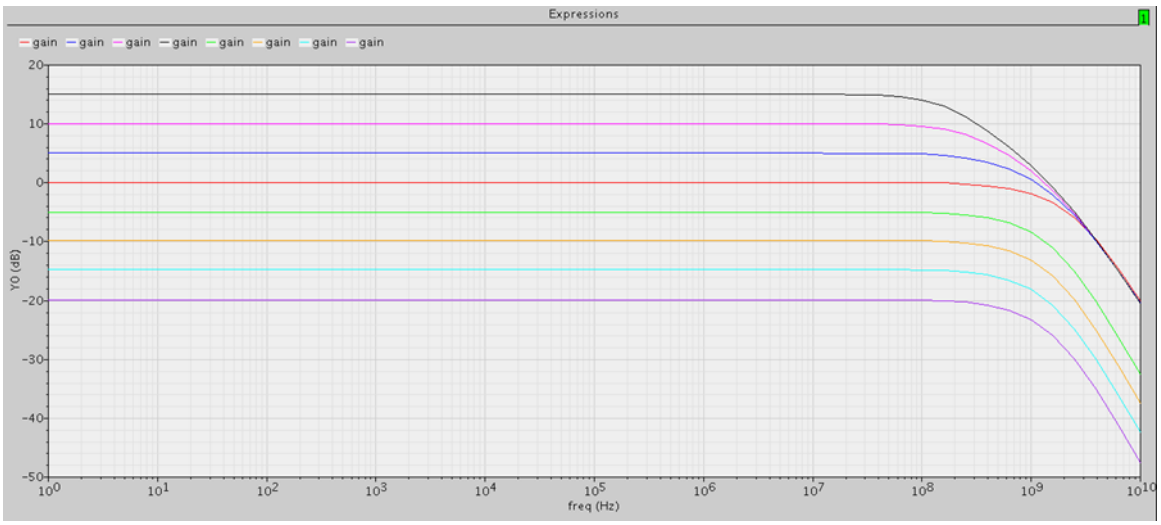

Figure 77: Frequency response of the VGA all gain levels

Alll gain levels has a bandwidth higher than 100MHz and the gain levels have no variation over the bandwidth for the gain of 15 dB the BW is 300 MHz at load capacitor is 300fF and for the low gain level -20 dB the BW $>$ 1GHz . The gain error is measured and it's less than 0.2dB.

Noise

As we stated before the noise can be considered as the input referred noise as this is the first stage so it has to have the best noise performance and to have high gain when working with the second and third stages so their input noise will be small when we refer it to the input because it will be divided by high gain stage .

The reason for having high noise at the low frequency is due to the flicker noise but as the frequency increases the noise contribution will be due to the thermal noise .The input referred noise for different gain values is shown in Figure 78.

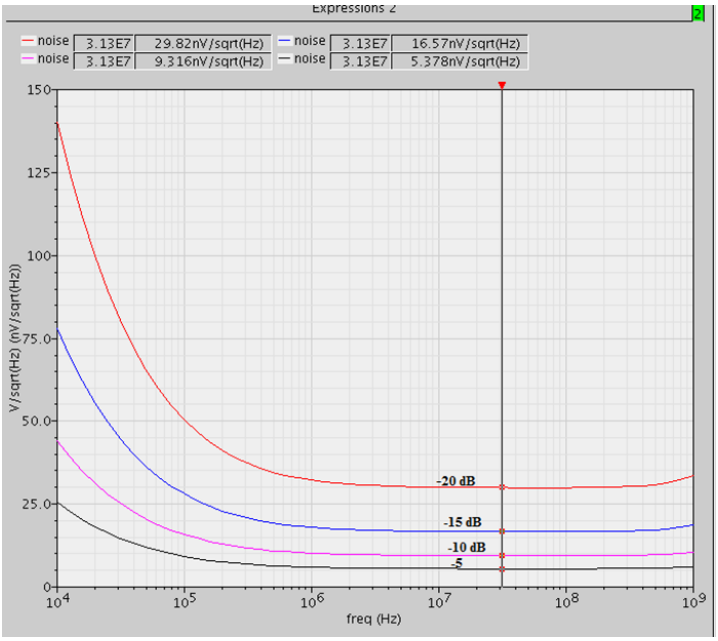

Figure 78: The input referred noise for different gain levels

The total noise in case of 0 dB gain level and when integrating it from 1MHz to 300MHz it reached the noise threshold at 110MHz accepted as shown in Figure 79.

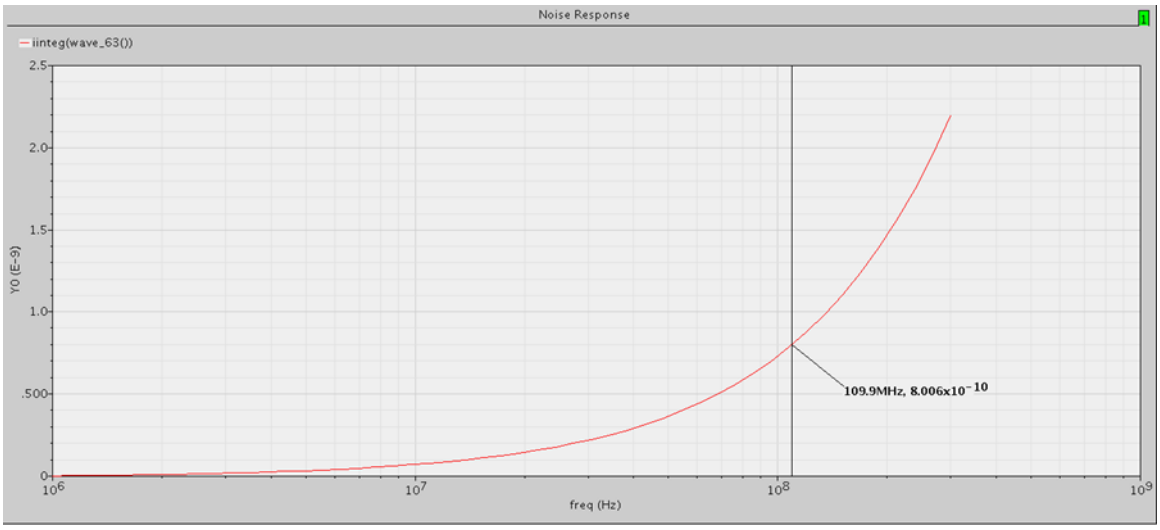

Figure 79: The total integrated input referred noise at 0 dB gain

Linearity

The linearity test was done by the PSS analysis engine . In Figure 80 we can see the fundamental power and the third order inter modulation power and we extrapolate the curves at input power of -20dBm while this analysis was done at gain of 0 dB the IIP3 was found to be 10.1 dBm.

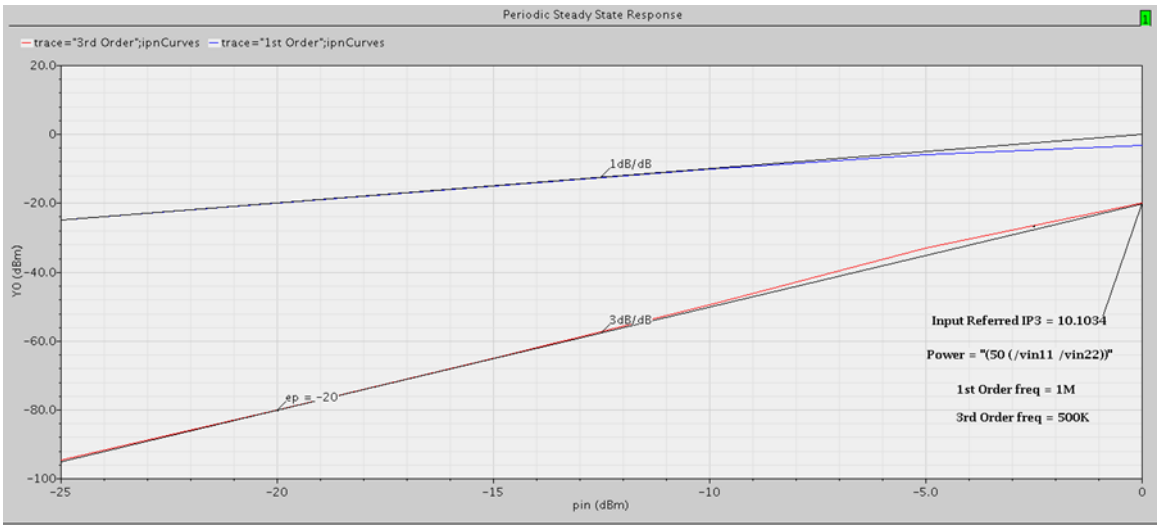

Figure 80: PSS analysis for IIP3 at 0 dB gain level

And the 1 dB compression point shown in Figure 81.

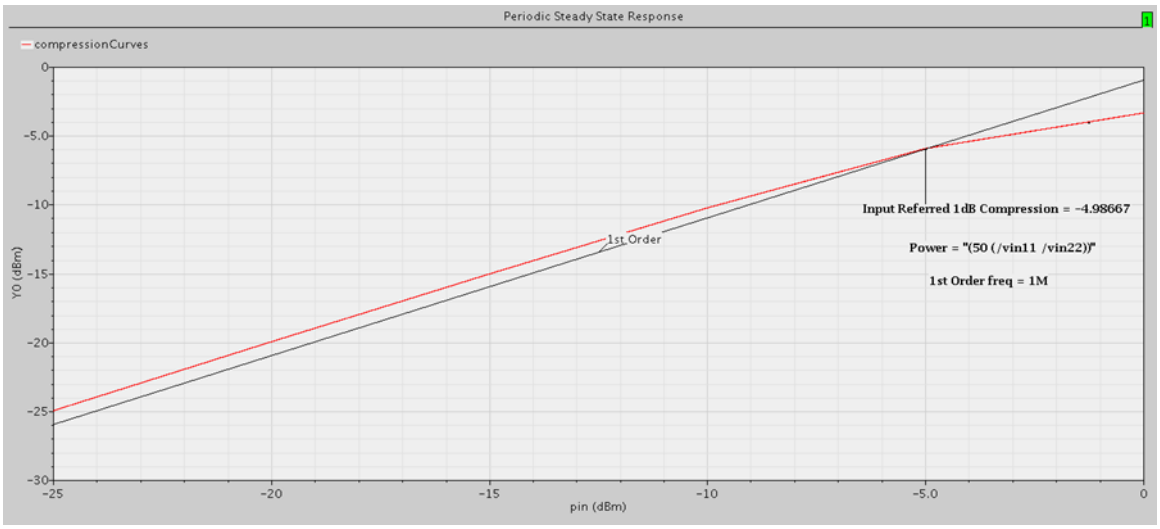

Figure 81: 1 dB compression point at 0 dB gain level

The different values for the IIP3 and 1 dB compression point at different gain values are listed in Table 20.

Table 21: VGA IIP3 and 1dBc for different gain settings

Gain	IIP3	1 dB compression point
-10	19.28 dBm	4.73 dBm
0	10.1 dBm	-4.95 dBm
10	8.25 dBm	-7.95 dBm
15	5.34 dBm	-12.69 dBm

Power consumption

The total power disspation of the first stage VGA is 5.66 mWatt.

Part V
Baseband Analog Filter

17 INTRODUCTION

The problem addressed here to be solved is the design of a continuous time analog filter. It's required to be a band-pass hopping filter. Throughout this section, a summary of the filter design process is going to be reviewed. Within such design process, a main bottleneck will arise which needs a solution. Such design bottleneck is going to be addressed through a proof-of-concept-example filter. That example's design, decision justifications, analysis, simulations, and results are going to be clarified as well.

18 FILTER DESIGN PROCESS

Any filter design process passes through three main steps. The first step is how to approximate a mathematical function that fulfills the required normalized specifications by the system in which the to-be-designed filter is going to be used. This step is called The Approximation Problem. Through this step, a design choice has to be made in order to determine which mathematical approximation is going to be used. As a matter of fact there are known types of mathematical approximations that have descending order requirement for same filter specifications. Approximations [1] are Butterworth, Chebyshev, Inverse-Chebyshev, and Elliptic. First one has the highest order and later ones descend for the same specified filter requirements as shown in Figure 82. However, first one has no ripples allover its response unlike its followers that have ripples in pass-band, stop-band, and both of them respectively. It's worth mentioning that the elliptic approximation often introduces an overhead which is the presence of extra zeros in the transfer function.

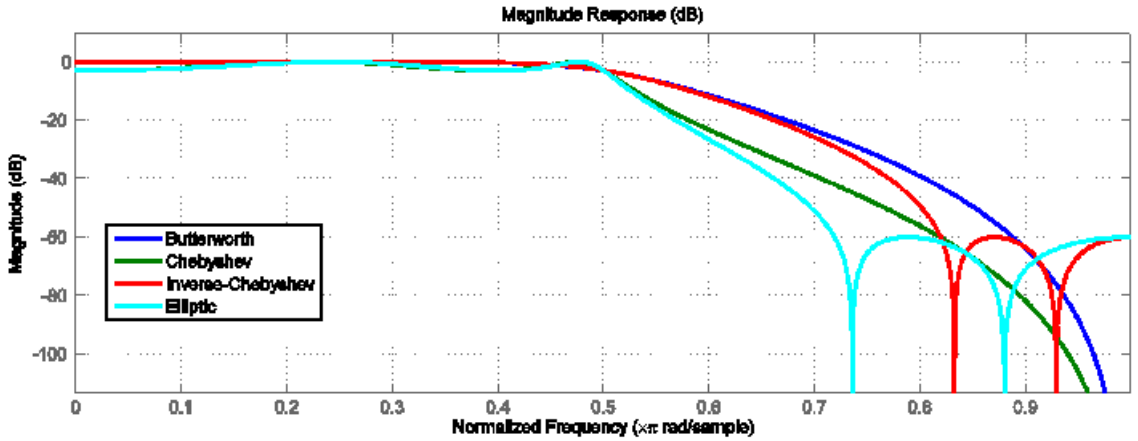

Figure 82: Different Aproximations for the same third order

After that, comes The Transfer Function Synthesis step. Frequency transformation is done here in order to create the required filter transfer function. On basis of such function, the required filter is going to be realized. Certain corner values in the filter response have to be mapped to transfer function coefficients so that it could be tuned and hopped easily. In other words, each coefficient's effect on the function response has to be determined.

Finally, a certain **Realization** has to be chosen from different filter circuit designs. Filters are realized on chip by several methods [2]. Two main approaches are the passive and active

circuits. On one hand, it's clear that we can't use passive one because it wouldn't provide high filter quality factors (Q). On the other hand, active filter circuits include four alternatives which are N-path, Q-enhanced LC, Switched Capacitors, and Gm-C filters.

- N-path filters may represent a good choice due its good linearity relative to others, high Q, tuning ability with clock frequencies eliminating the need to Q and w_o control circuits in other alternatives, and independency of Q on Dynamic Range (DR). However such alternative is rejected because of its dependence on clocks in tuning from the hopping point of view. That's because clocks' settling times are in the range of (4-5) usec [3] in addition to the used mixers' complexities. Also more consumed power than other circuits except for the Q and control circuits but such circuits may be activated on chip startup only (Foreground Calibration).

- Q-enhanced LC filters are an excellent choice regarding linearity. However, they are very poor in tuneability and DR.

- On one hand, switched Capacitors filters introduce solutions to the process variation problem as their parameters depend on capacitors' ratios which may control error within 0.1% [4]. On the other hand, their usage is limited only to low frequency signals because their controlling clock frequencies have to be less than dealt signals' highest frequencies by (20-200) times while such clock frequencies are in the range of 100 kHz to 2 MHz.

- Gm-C filters represent the best choice regarding tuneability and high frequency ranges. As a matter of fact the main challenge in our design is the hopping feasibility which is reflected, by turn, on tuneability. It's worth mentioning that their design include vigorous trade-offs among frequency range, DR, Q, and dissipated power. They will be overcome in the design which will impose complexity to it.

From the above discussion, it's clear that the best choice for filter circuit realization is the Gm-C ones in the case addressed throughout this work. It appears also that the filter design process is a systematic approach which has a main bottleneck. Such bottleneck arises in the tradeoffs among different qualities fulfilled by the circuit. A lot of compromises, classifications, and balances have been addressed in previous work [5], [6], [7], and [8]. However, the hopping dilemma hasn't been addressed directly for a whole Gm-C filter before. It's meant by the hopping dilemma is the tradeoffs between the settling time of different filter components and other qualities fulfilled by the filter, i.e. power, linearity, Q, DR... etc. This work's main focus is to address such quality, hopping rate and circuit settling time, by studying a prototype circuit.

19 PROTOTYPE FILTER

It's required to design a low-pass filter (LPF) capable of hopping and devise a method to test such settling. So, a second order LPF is going to be created using Gm-C circuits approach as discussed before. It's expected to have it low-passing frequencies under either 10 MHz or 50 MHz.

19.1 Architecture

A fully differential architecture is used. It's an architecture based on the fully differential basic integrator building block as shown in Figure 83. As it appears the main relation governing input (i/p) and output (o/p) of such cell is:

$V_0 = V_i/sC$

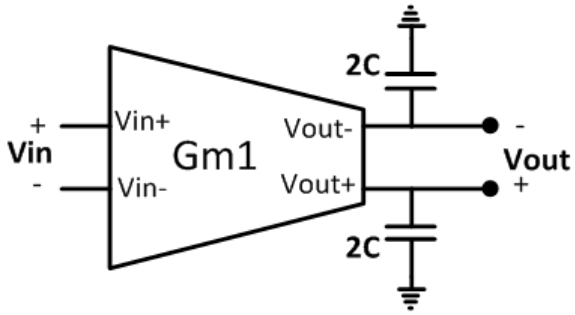

Figure 83: Basic Integrator Cell in Gm-C Architectures

The filter system block diagram is as shown in Figure 84.

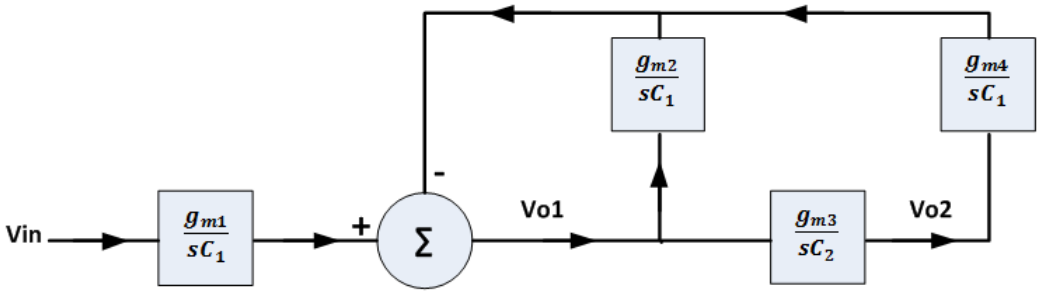

Figure 84: Prototype Filter System Block Diagram

Therefore the filter schematic is as shown in Figure 85.

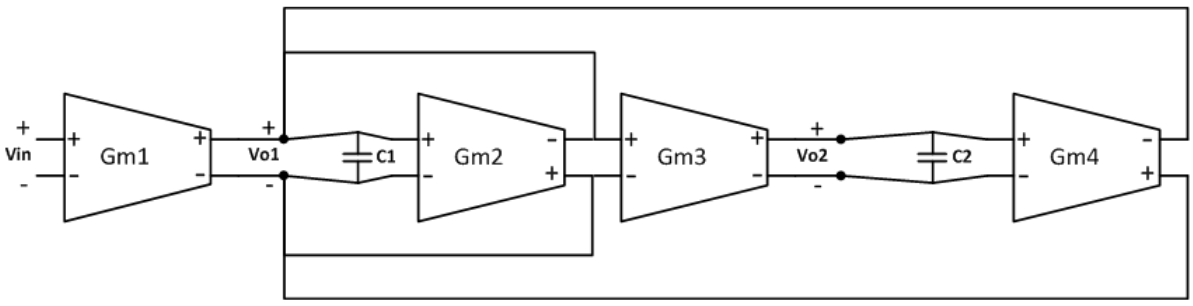

Figure 85: The Filter Preliminary Circuit Schematic

19.2 Circuit Analysis

So the i/p o/p relationships are as follows

$$V_{O1} = V_{in}.\frac{g_{m1}}{sC_1} - V_{O1}.\frac{g_{m2}}{sC_1} - V_{O2}.\frac{g_{m4}}{sC_1}$$

$$V_{O2} = V_{O1}.\frac{g_{m3}}{sC_2}$$

$$\frac{V_{O1}}{V_{in}} = \frac{s.\frac{g_{m1}}{C_1}}{s^2 + s.\frac{g_{m2}}{C_1} + \frac{g_{m3}.g_{m4}}{C_1.C_2}}$$

$$\frac{V_{O2}}{V_{in}} = \frac{\frac{g_{m1}.g_{m3}}{C_1.C_2}}{s^2 + s.\frac{g_{m2}}{C_1} + \frac{g_{m3}.g_{m4}}{C_1.C_2}} \quad \text{..... (Eq. 5)}$$

As it appears, this work interest is in Eq. 5 which represents the transfer function for a 2nd order LPF that can be tuned through tuning either its cut-off frequency.

$$\omega_c = \sqrt{\frac{g_{m3}.g_{m4}}{C_1.C_2}}$$

Or Its quality factor:

$$Q = \sqrt{\frac{g_{m3}.g_{m4}.C_1}{C_2}}.\frac{1}{g_{m2}}$$

19.3 Tuning/Hopping Technique

There are a lot of tuning techniques for the used gm's in the circuit as mentioned in [5]. Since this work seeks a proof-of-concept for the hopping concept feasibility in the filter circuit, therefore a vigorous different hopping technique is used. It's direct switching between two different tracks as shown in Figure 86. Such technique represents worst hopping choice regarding all circuit qualities. So, it surely proves the hopping concept feasibility.

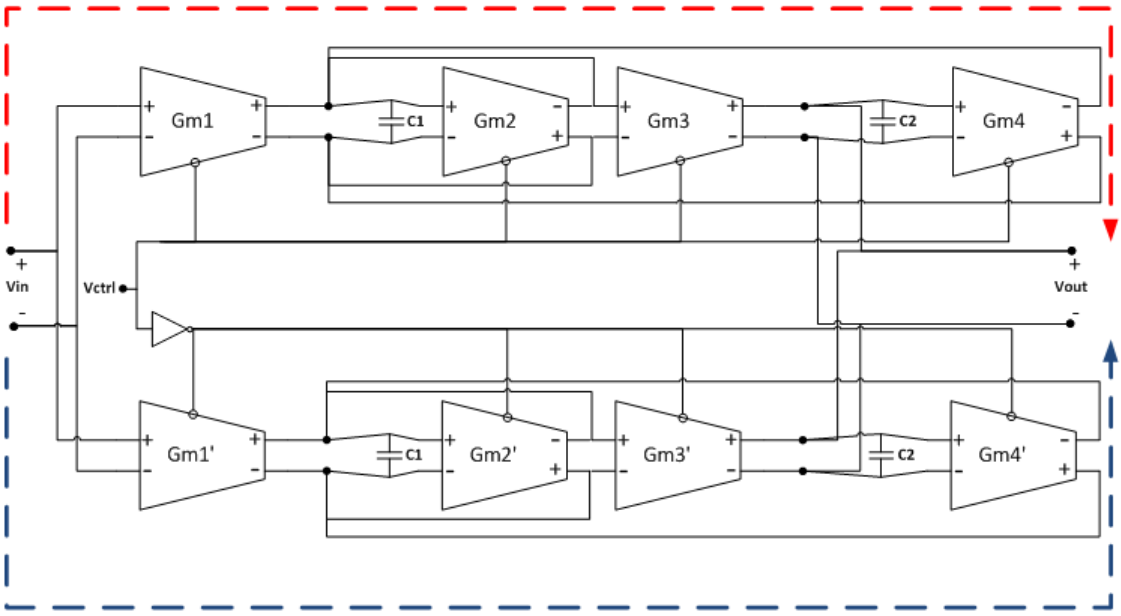

Figure 86: Full Prototype Filter Schematic Including the Switching Scheme

19.4 The Used Gm Cell

A heavily source degenerated cell is used in order to have better linearity [9]. Of course, that's not the only technique enhancing linearity but hopping is the main quality addressed in this

stage. The used Gm cell architecture along with its common-mode feedback (CMFB) circuit is shown in Figure 87.

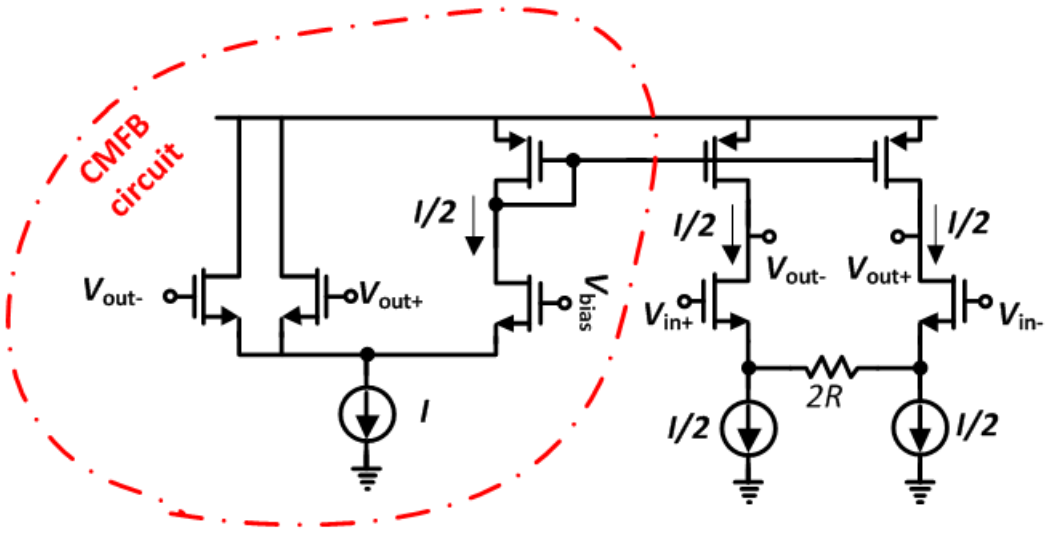

Figure 87: Used Gm Cell Architecture and the Used CMFB

20 HOPPING TEST

The main problem in testing hopping is how to run simultaneous analyses in the used simulation tool. That's because hopping among different frequency responses is undergone in time-running environment by its nature. In other words, it's needed to simulate the frequency response of the system at each hopping instant. Such need implies running simultaneous frequency domain analysis and transient one as well in order to figure out after how long time the filter settles on the 10 MHz response as shown in Figure 88 or on the 50 MHz response as in Figure 89.

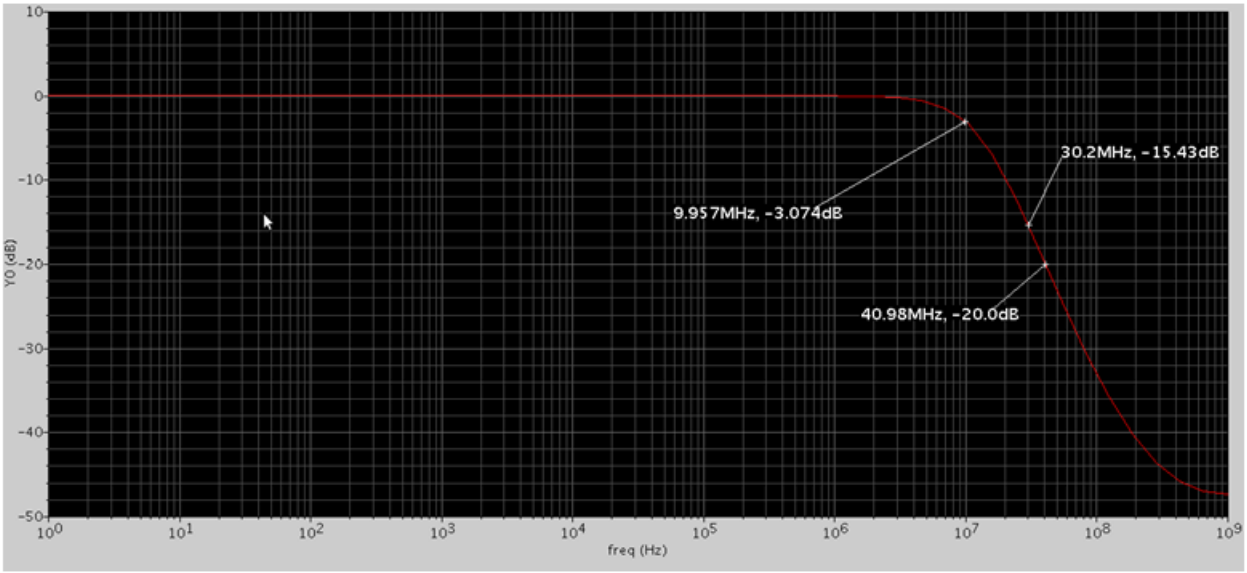

Figure 88: 10-MHz Cut-off Filter

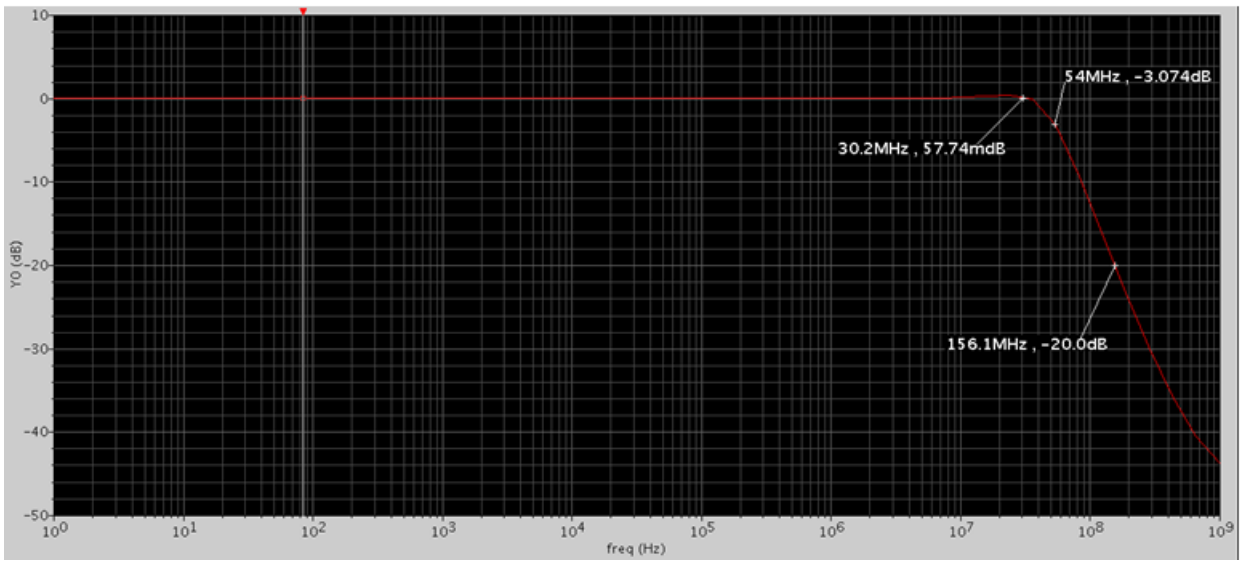

Figure 89: 50-MHz Cut-off Filter

20.1 Option 1

The first solution is to use transient analysis to test the i/p o/p relation of the filter on a sinusoidal i/p signal at a certain frequency. That's done through tracking the attenuation level applied to the i/p signal at each instant of time. So, if the applied i/p sinusoidal signal is at an intermediate frequency between the two responses of the filter, it will be passed a whole in case of one response and attenuated in the other case. Therefore, 30 MHz is chosen as a testing frequency. The i/p differential signal is chosen to have maximum voltage level 0.2 V so that all working Gm cells operate in their tuned transconductance levels. Consequently, from the attenuation level applied to a 30 MHz signal appearing in Fig. 88 it's expected that the o/p signal maximum level V_m is either V_m=0.2 V in the case of the 50 MHz response or V_m=0.2*10^((-15.43)/20)=0.0338 V. That appears obviously in Figure 90.

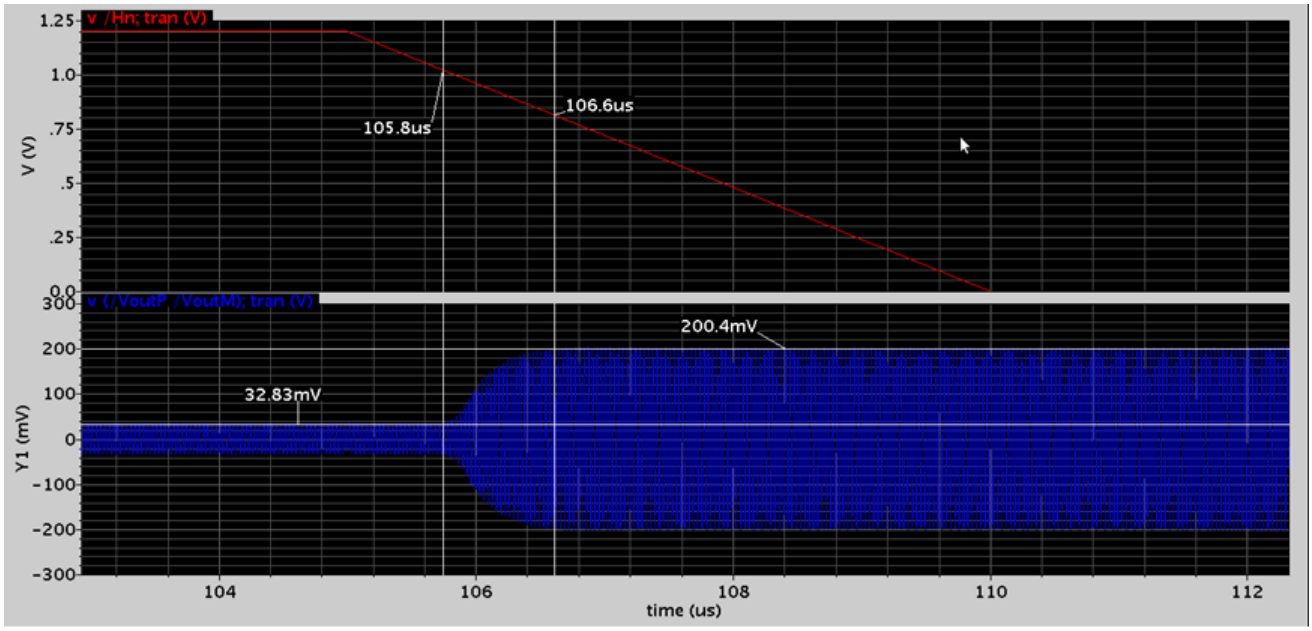

Figure 90: Filter O/P for a 30 MHz I/P Sinusoidal Signal During Hopping Transition Through Hn Control Signal

One can say that the settling time of the filter appears from Fig. 90 to be 800 ns. However, this is half of the truth only because such settling time is that of the transition from 10 MHz to 50 MHz response. What about the 50 MHz to 10 MHz transition settling time? The answer to this question appears in Figure 91 which shows that such settling time is 5.37 us although the control signal has less transition interval than that in case of Figure 91.

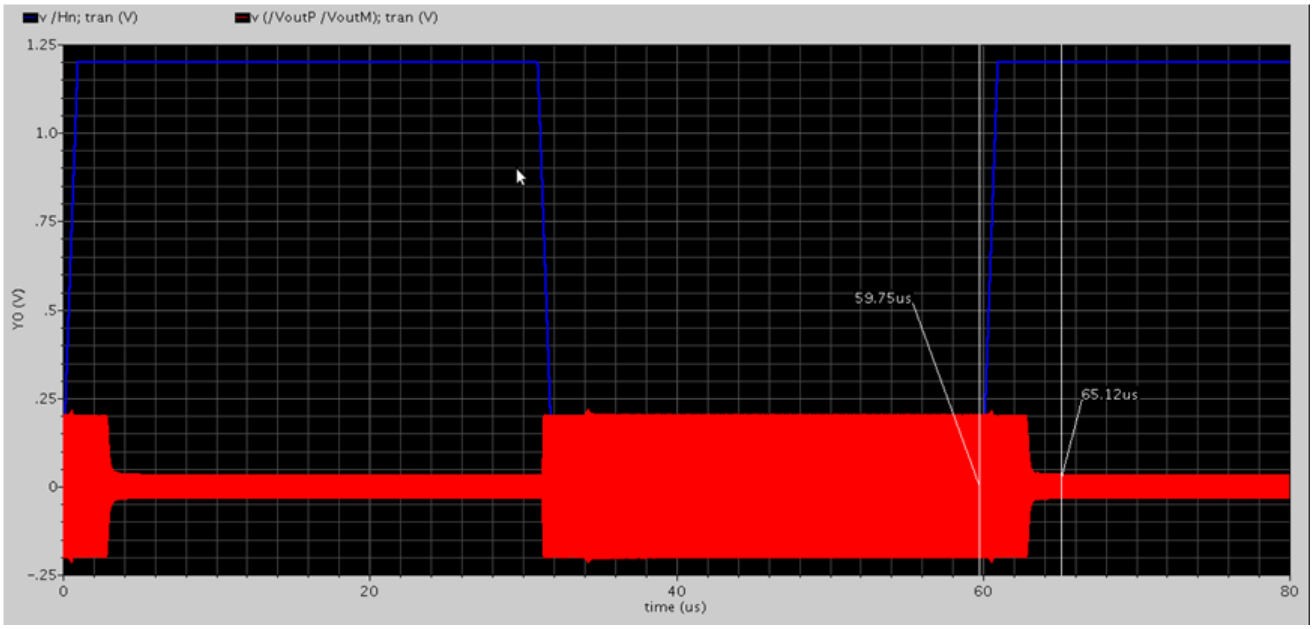

Figure 91: Filter O/P for a 30 MHz I/P Sinusoidal Signal During Hopping Transition Through Hn Control Signal

20.2 Option 2

The second solution is considered a novel technique for such test. It depends taking the frequency response of the filter each 1 us so that a 3 dimensional (3D) curve can be generated. An impulse is applied to the filter i/p each μsec, i.e. a train of impulses is applied to it along the whole transient analysis. The reason behind choosing impulse is its frequency domain representation which is a constant along the frequency axis. So, each 1 μsec the o/p signal's time samples are Fourier transformed as well as the i/p impulse time samples. Then the frequency response within this 1 μsec can be generated through dividing both results or subtracting their decibel scale values. The resulted 3D curve is shown in Fig. 92. By studying this 3D curve, previously mentioned settling times are verified as well as the whole filter response not only its response to a signal frequency as in option 1.

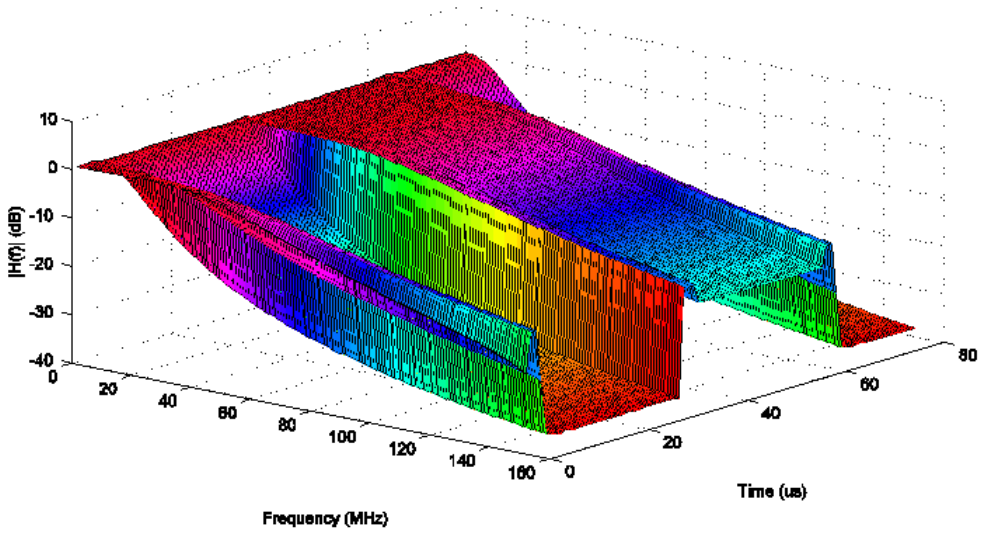

Figure 92: Prototype Filter 3D Response Curve

Appendix: Hopping Testing 3D Curve Generation MATLAB Code

.

```
clear all;
data=xlsread('pulseIn');
clc;
close all;
t=data(:,1)*1e6;
Vin=data(:,2);
Vout=data(:,3);
Hn=data(:,4);
plot(t,Hn,t,Vin,t,Vout)
xlabel('Time (us)')
ylabel('Hn, Vin, Vout (V)')
legend('Hn','Vin','Vout') figure;
Fs = 2e9; % Sampling frequency
T = 1/Fs; % Sampling time
NFFT=2048; tdraw=20;
X = fft(Vin((tdraw-1)*2000+1:tdraw*2000),NFFT)/2000;
f = 1e-6*Fs/2*linspace(0,1,NFFT/2+1);
ind=find(f>150);
freq=f(1:ind(1));
for tstep=1:80
Y = fft(Vout((tstep-1)*2000+1:tstep*2000),NFFT)/2000;
TF_t_f(tstep,:)=20*log10(abs(Y(1:ind(1)))./abs(X(1:ind(1))));
clear Y;
end
tt=1:80;
[t_mesh,f_mesh]=meshgrid(tt,freq);
surf(f_mesh,t_mesh,TF_t_f')
colormap hsv
```

```
xlabel('Frequency (MHz)')
ylabel('Time (us)')
zlabel('|H(f)| (dB)')
```

21 REFERENCES

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