Analog Integrated Circuits
Lecture 1: MOS Physics

ELC467 – Spring 2014

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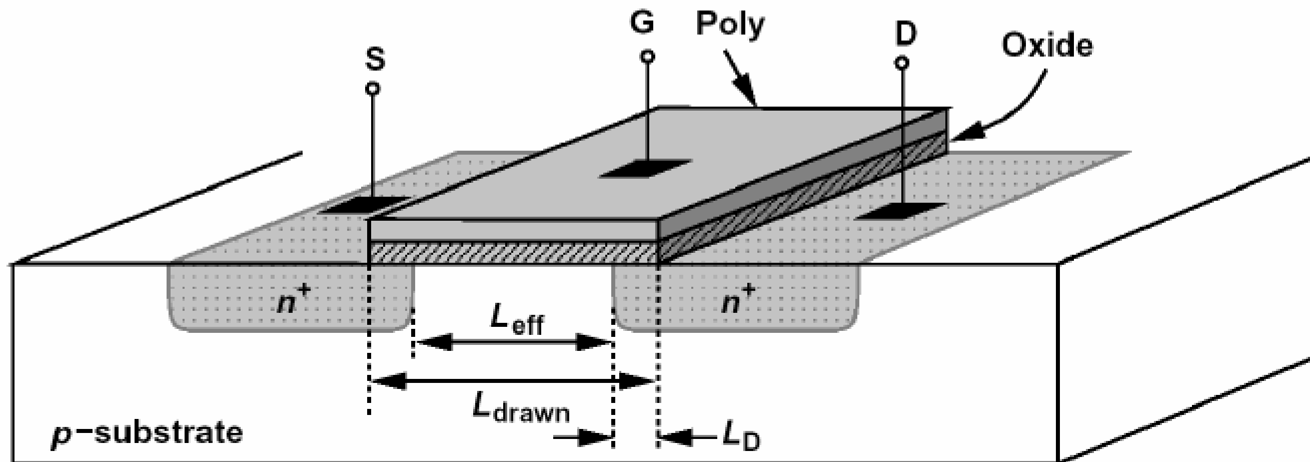
MOS Structure



- A piece of polysilicon with a width of W and length of L on top of a thin layer of oxide defines the gate area.
- Source and drain areas are heavily doped.
- Substrate usually tied to the most negative voltage.
- Leff = L – $2L_D$, where L_D is the side diffusion of source and drain.

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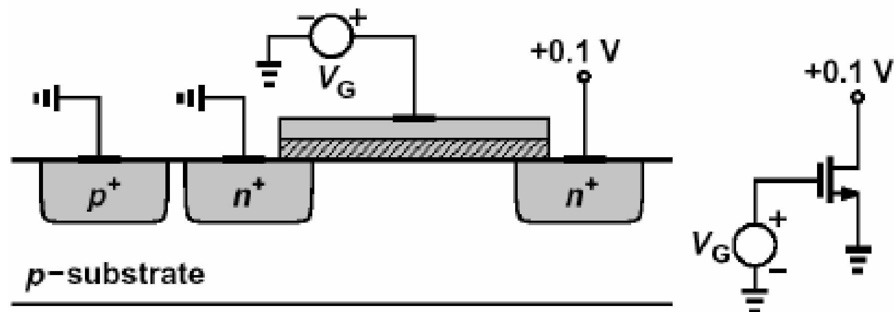
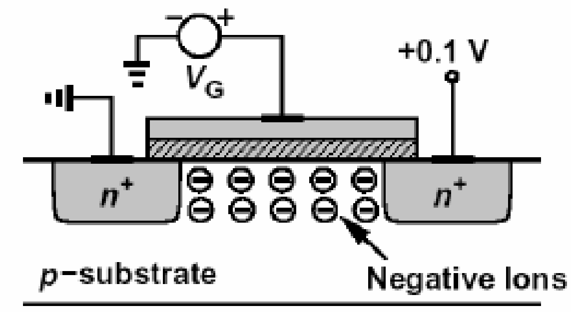
MOS characteristics – Threshold Voltage



(a)



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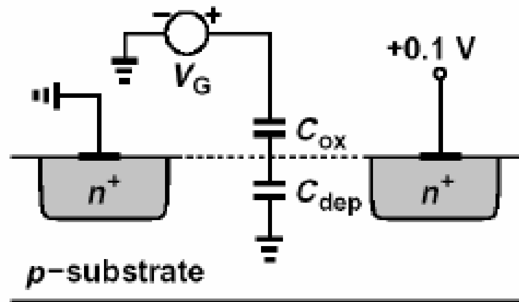

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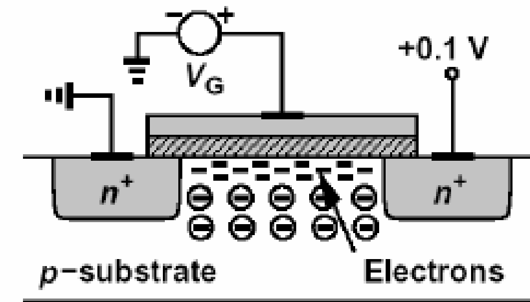

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MOS characteristics – Threshold Voltage

- For $V_{GS} < V_{TH}$, holes in substrate are repelled from gate area, leaving negative ions behind. (No current flows because no carriers are available.) A depletion region forms under the gate.
- For $V_{GS} \approx V_{TH}$, electrons are attracted to the interface under gate, establishing a “channel” for conduction. The channel is also called the “inversion layer.”
  - $Q_{inv} = C_{ox}WL(V_{GS} - V_{TH})$
  - $C_{ox} = \frac{\epsilon_{si}}{t_{ox}} \quad \Rightarrow \frac{capacitance}{area\ of\ oxide}$
- For $V_{GS} \approx V_{TH}$, depletion region under channel remains relatively constant, but the charge in inversion layer increases.
- Surface (substrate) potential must drop $2\phi_F$ below gate potential to start inversion (If $V_{source} = 0$).
- Turn-on process not really abrupt, i.e., for $V_{GS} \approx V_{TH}$, $I_D > 0$. => Sub-threshold conduction (considered later).

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MOS characteristics – Threshold Voltage

- For a a long-channel device with uniform substrate doping: (and $V_{SUB} = V_{SOURCE}$):
  - $V_{TH} = \phi_{MS} + 2\phi_F + \frac{Q_{dep}}{C_{ox}}$
  - $\phi_F = \frac{kT}{q} \ln \frac{N_{sub}}{n_i}$
  - $Q_{dep} = \sqrt{4q\epsilon_{si}|\phi_F|}$
- Note: There is no importance for the absolute value of the G-S voltage. But the important term is "$V_{GS} - V_{TH}$" (Effective Gate voltage "V_{eff}" or Overdrive voltage "V_{od}").

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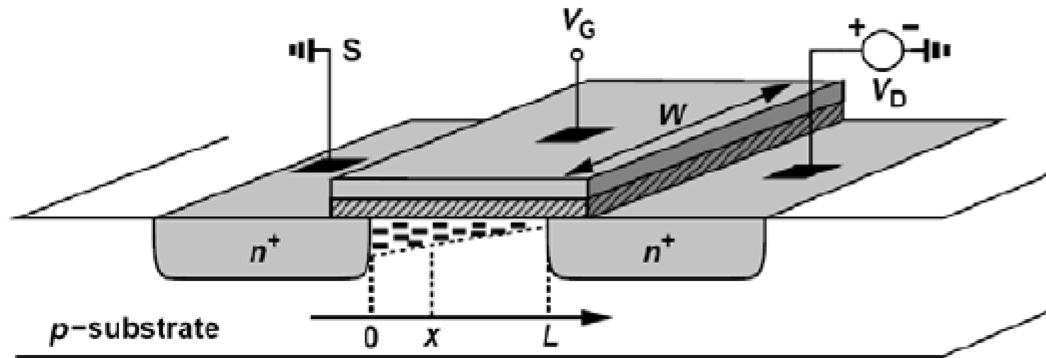
MOS I-V characteristics



- For $V_{GS} > V_{TH}$, current flows between source and drain by drift (Resistive current).
- This is a voltage-dependent (nonlinear) resistor.
- $I_D = \frac{Q_{inv}}{\tau_T}$
  - τ_T: Transit time through inversion layer from Source to Drain.
- For low V_{DS},
  - $I_D = \mu C_{ox} \frac{W}{L}(V_{GS} - V_{TH})V_{DS}$

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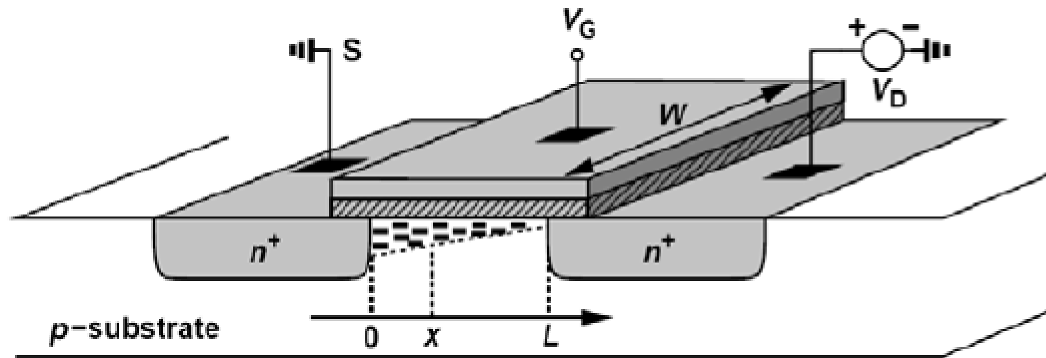
MOS I-V characteristics



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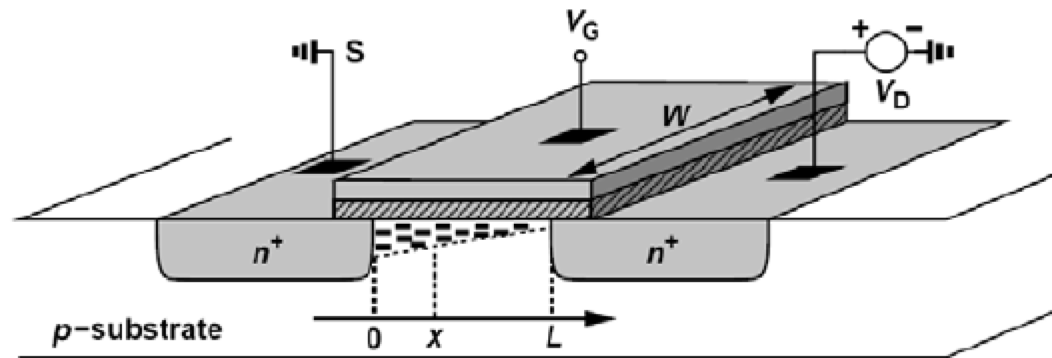
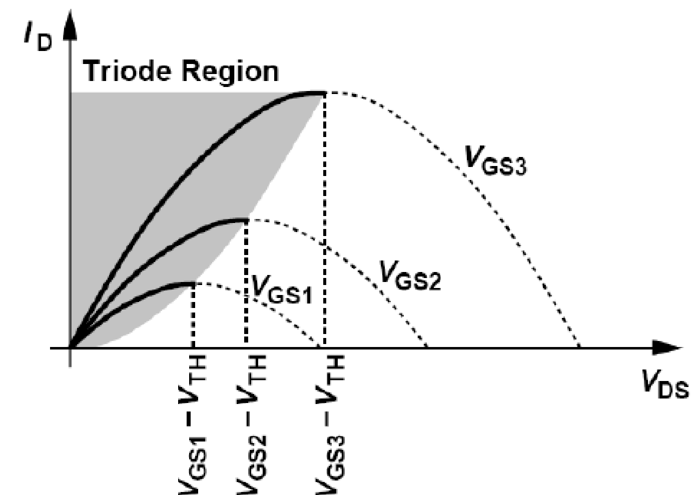
MOS I-V characteristics



- For higher V_{DS} (General Formulas)
  - find the current, multiply charge density by charge velocity.
  - $I_D = WC_{ox}[V_{GS} - V(x) - V_{TH}]\mu_n \frac{dV(x)}{dx}$
  - $I_D = \mu_n C_{ox} \frac{W}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2]$



- $R_{on} \cong \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})}$

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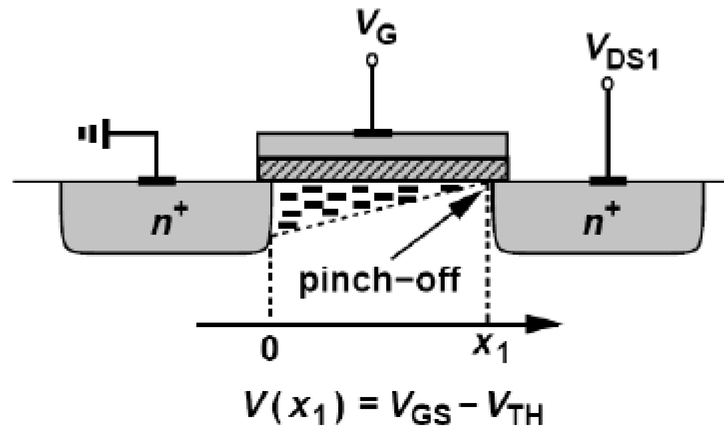
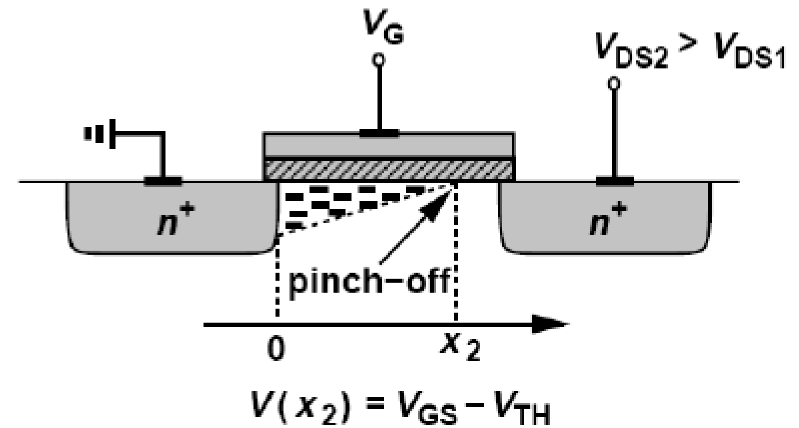
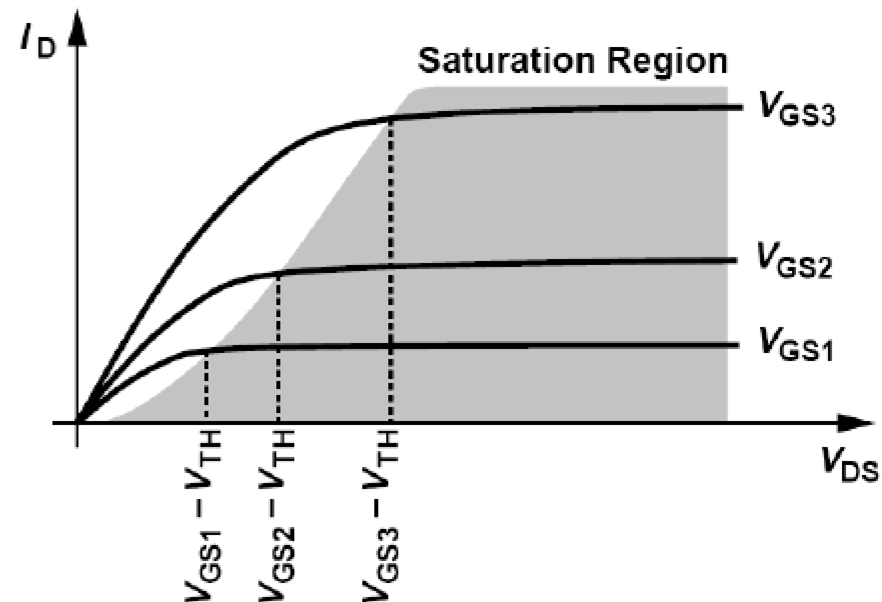
MOS I-V characteristics





- What happens if $V_{DS} > V_{GS} - V_{TH}$?
  - Electrons reach a high velocity near the end of inversion layer and shoot into depletion region around the drain.
  - $V_{GD} < V_{TH} \rightarrow$ Inversion layer at drain vanishes. But current continues to flow.
  - Voltage at pinch-off = $V_{GS} - V_{TH}$



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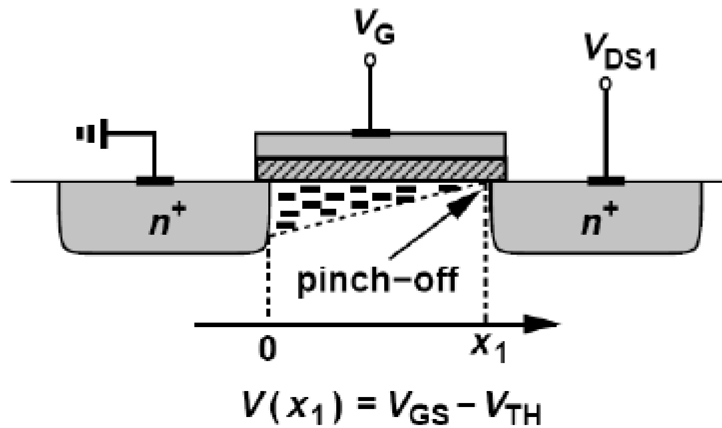
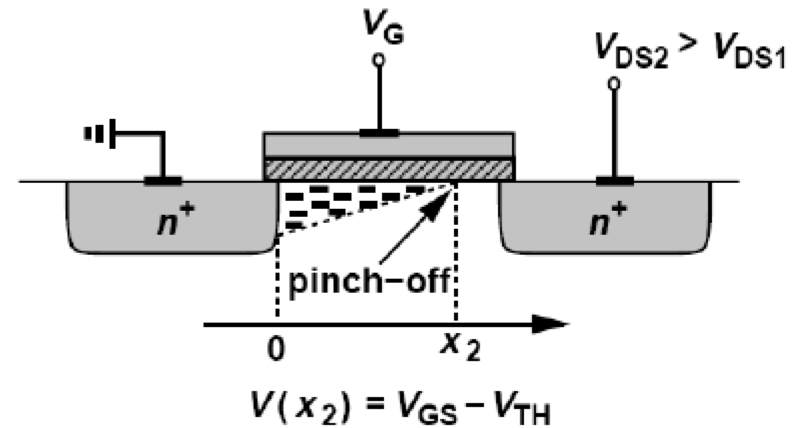
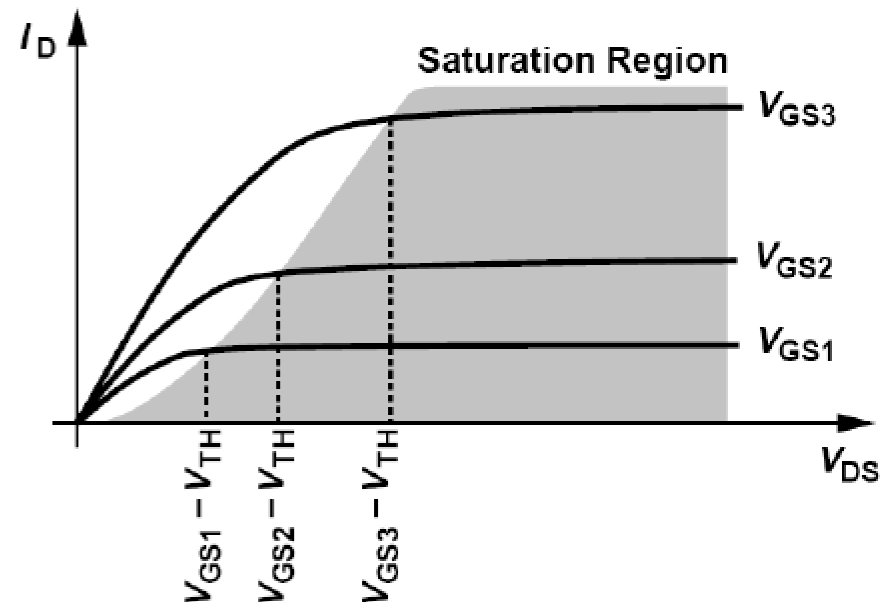
MOS I-V characteristics





- Voltage across the inversion layer is fixed (independent of the V_{DS}) from that point on.
- Depletion region from the pinch-off point to the drain.
- Device enters **"Saturation Region"**.
- $I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{eff}^2$ (quadratic)



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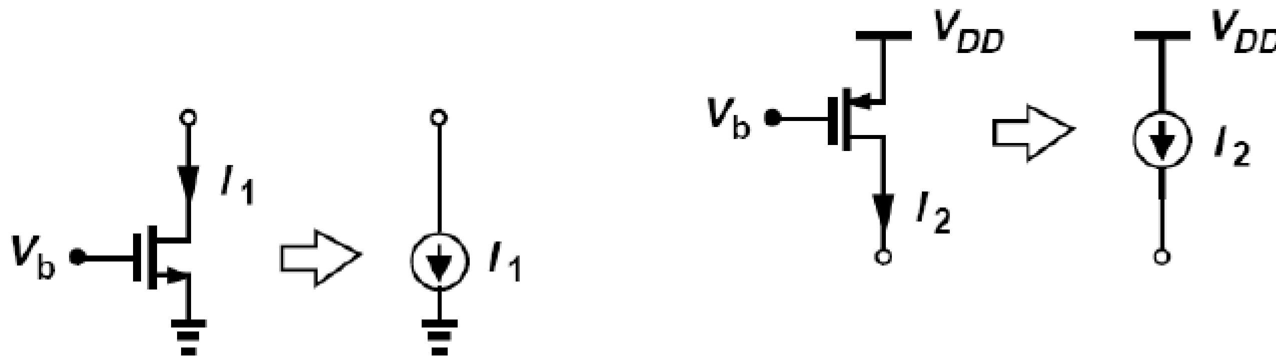
MOS: In Saturation

- In saturation, I_D is independent of V_{DS}



- $R_{out} = \infty$
- $G_{out} = 0$

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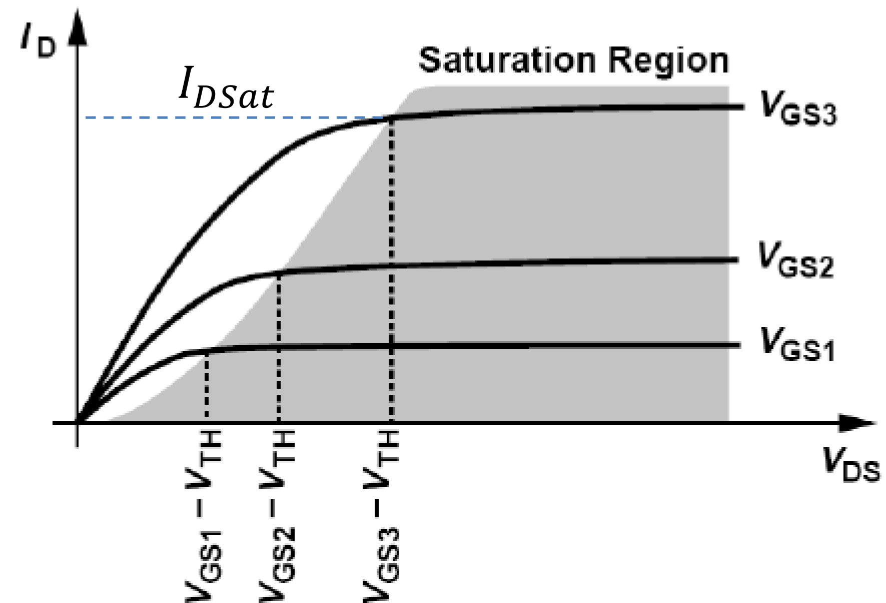
MOS: Channel length modulation

- Channel length modulation by V_{DS} causes the saturation current to varry with V_{DS}.
  - $\frac{\partial I_D}{\partial V_{DS}} = \frac{\partial I_D}{\partial L} \times \frac{\partial L}{\partial V_{DS}} = \frac{I_{DSat}}{\alpha L \sqrt{V_{DS} - V_{eff}}}$
  - Where: $\frac{\partial L}{\partial V_{DS}}$: Depletion region modulation.
  - $\alpha = \sqrt{\frac{q N_{dop}}{2 \epsilon_{si}}}$
  - $\frac{\partial I_D}{\partial V_{DS}} = \frac{I_{DSat}}{\alpha L \sqrt{V_{DG} + V_{TH}}}$
    - Non-zero o/p conductance



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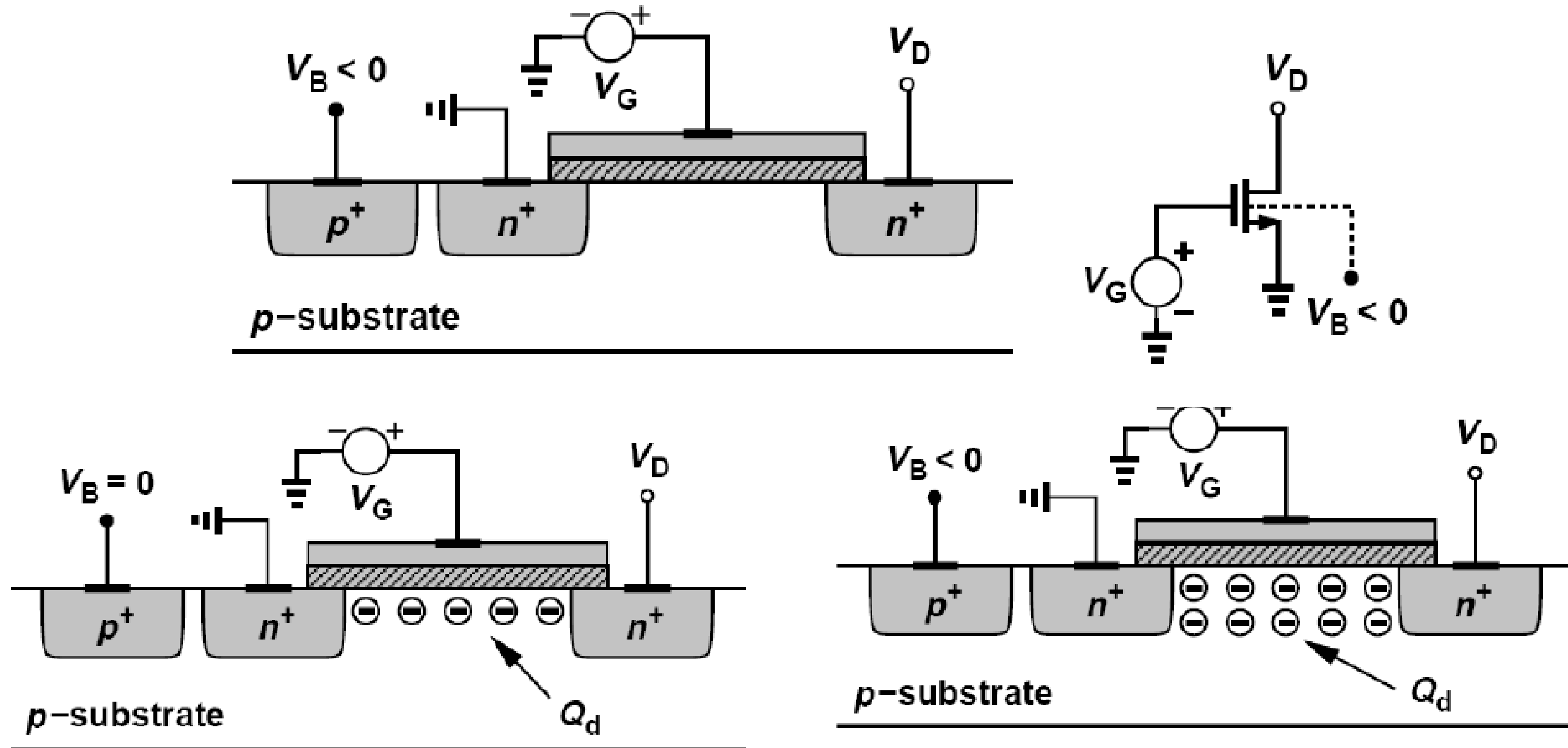
MOS: Substrate or Body Effect



- With V_{SB} present, we need larger V_{GS} to drop $(2\phi_F - V_{SB})$ across the depletion region at onset of inversion. → i.e. V_{TH} is larger.
- $V_{TH} = V_{TH0} + \gamma[\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}]$ and $\gamma = \sqrt{2q\epsilon_{si}N_{sub}}/C_{ox}$

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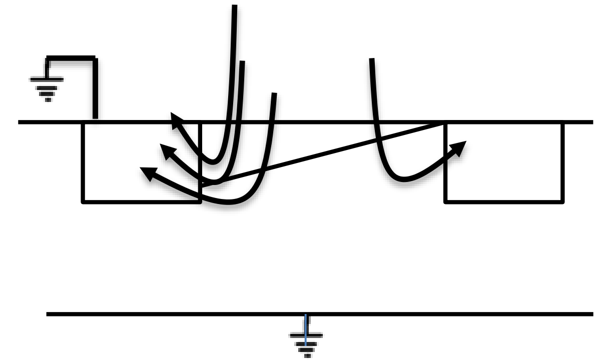
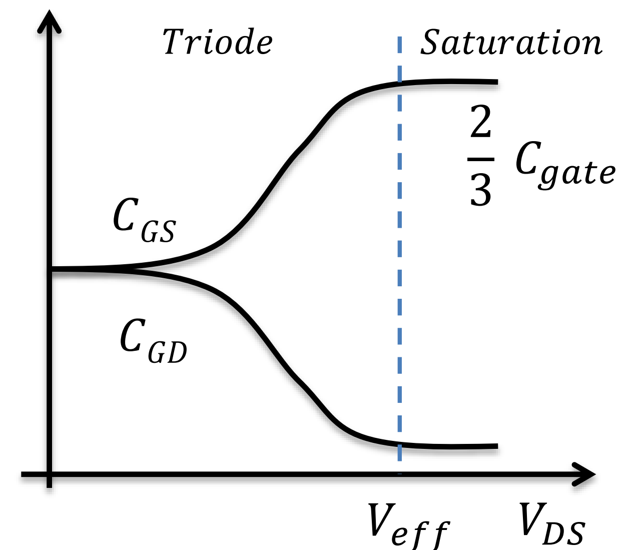
MOS: Intrinsic Capacitance

- Capacitance is always defined as small-signal around a bias point:
  - $C_{SS} \triangleq \frac{\partial Q}{\partial V}|_{Bias}$
- At $V_{DS} = 0, C_{gate} = C_{ox}WL = C_{GS} + C_{DS}$, both equal independent of V_{GS} above V_{TH}.
- Increasing V_{DS}, due to the non-uniform inversion layer, more charges tend to move toward the source than towards the drain, $C_{GS} \uparrow$ and $C_{DS} \downarrow$.





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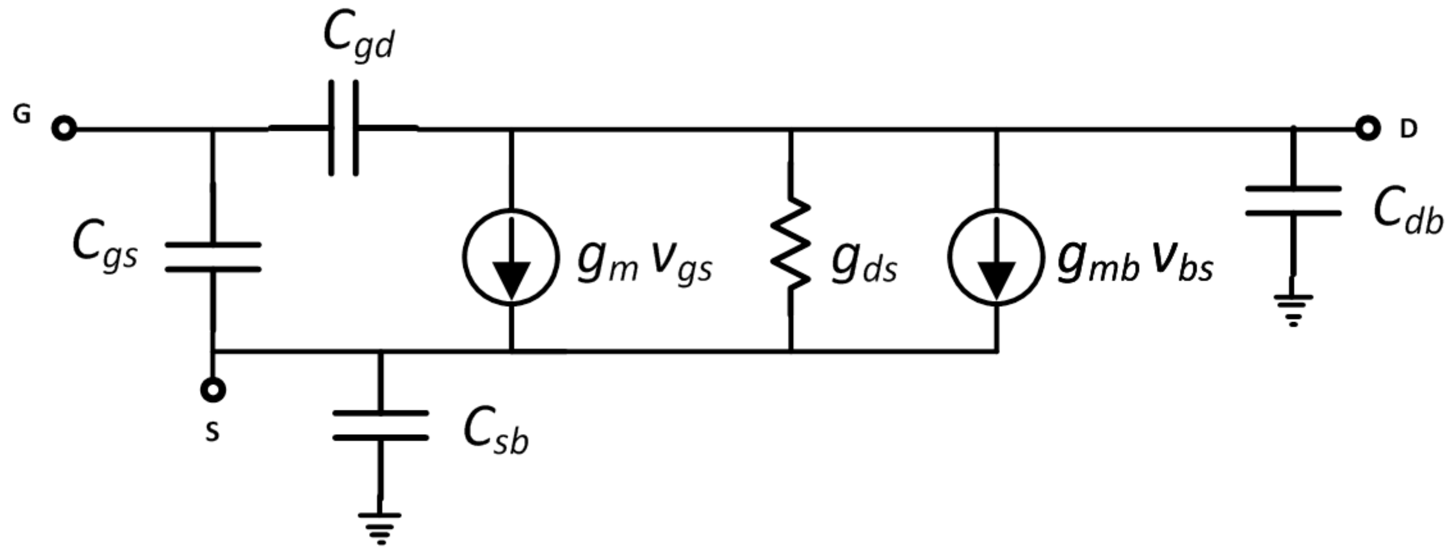
Small-Signal Model



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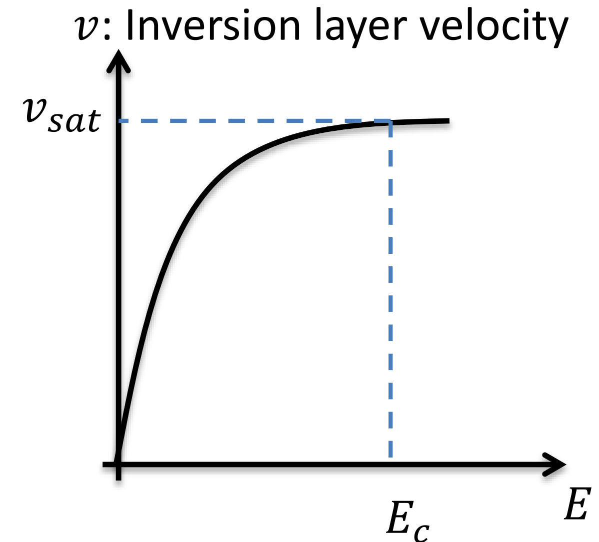
Deep Sub-Micron Technologies – Velocity Saturation

- What's the effect of reducing the L?
- Transit time:
  - $\tau_T = \frac{L}{v(velocity)} = \frac{L}{\mu_n E} = \frac{L}{\mu_n(\frac{V_{DS}}{L})} = \frac{L^2}{\mu_n V_{DS}}$
  - Shrinking L makes the transistor faster 4x.
  - For electronics in Si: $v_{sat} = 10^5 m/s$ and $E_c = 1.5 \times 10^6 V/m$
- As we approach v_{sat}, the expression for mobility changes:
  - $\mu = \frac{\mu_0}{1+\frac{V_{eff}}{E_c \times L}}$
  - $I_{DSat} = \frac{1}{2} \frac{\mu_0}{1+\frac{V_{eff}}{E_c \times L}} C_{ox} \frac{W}{L} V_{eff}^2 \cong \mu_0 W C_{ox} v_{sat} V_{eff}$ (Linear)



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Deep Sub-Micron Technologies – Velocity Saturation

- With velocity saturation taken into account, FET enters saturation at $V_{DS} \cong V_{eff}(1 - \frac{V_{eff}}{2E_c L})$

- For long channels, $\tau_T = \frac{L^2}{\mu V_{eff}}$

- For short channels, $\tau_T = \frac{L}{v_{sat}}$

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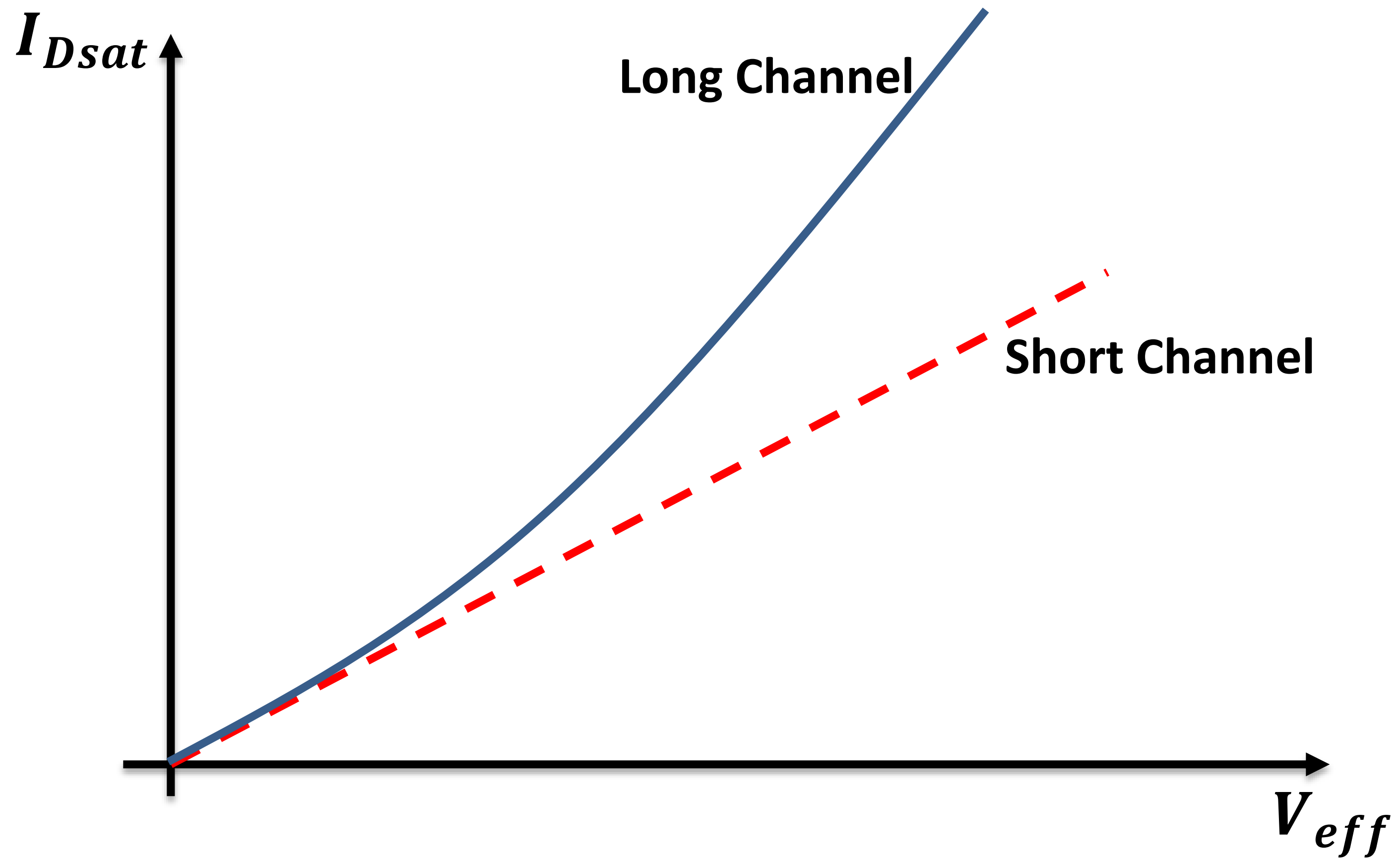
I_{Dsat} versus V_{eff}



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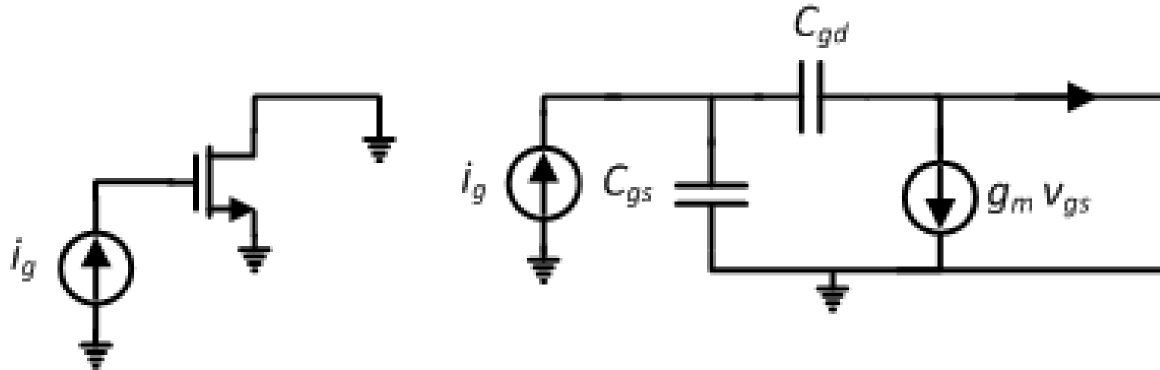
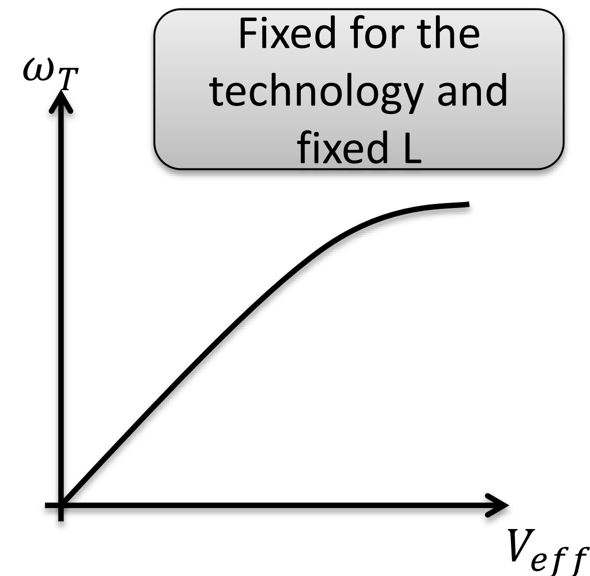
Circuit Implications of τ_T



- $i_d = \frac{i_g \times g_m}{j\omega(C_{gs}+C_{gd})} \cong \frac{i_g \times g_m}{j\omega C_{gate}}$
- $\left|\frac{i_d}{i_g}\right| = \frac{g_m}{\omega C_{gate}}$
- Current gain is 1 when $\omega = \omega_T = \frac{g_m}{C_{gate}}$
- For long channels, $g_m = \frac{2I_D}{V_{eff}}$
- $\Rightarrow \ \omega_T = \frac{\mu C_{ox}\frac{W}{L}V_{eff}}{C_{ox}WL} = \frac{\mu V_{eff}}{L^2} = \frac{1}{\tau_T}$
- ω_T is fundamentally the highest frequency where any transistor can amplify.

Low-voltage – High-Speed trade-off



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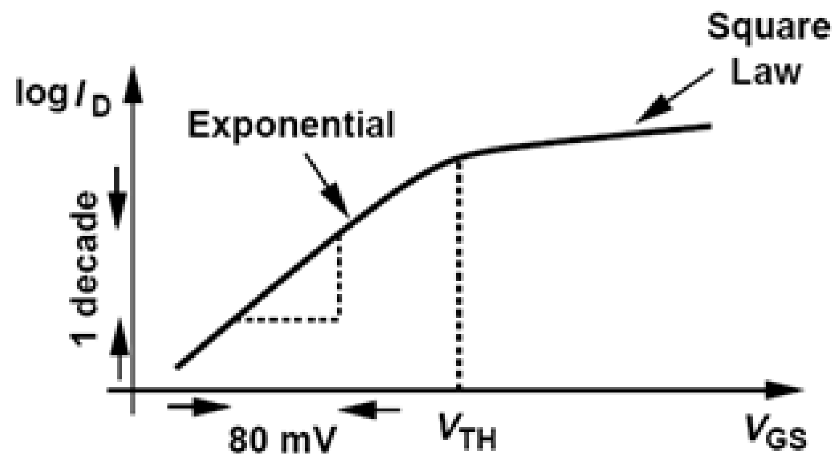
MOS: Subthreshold

- Subthreshold Conduction:

For V_{GS} near V_{TH}, I_D has an exponential dependence on V_{GS}:

$$I_D = I_0 \exp \frac{V_{GS}}{\zeta V_T}$$



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Homework #1

- Using Cadence and using the circuit in Slide 20, sketch "ω_T versus V_{eff}" for the transistors nmos1v, pmos1v, nmos3v and pmos3v.
  - Note: you need to bias the circuit properly. Slide 20 only shows the AC part of the circuit.
  - Repeat the experiment for each transistor for different "L" values (L_{min}, $2L_{min}$ and $4L_{min}$)
- Make any necessary assumptions.

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