Selected Topics in Analog Integrated Circuits
Lecture 1: Weak Inversion Operation

ELC701A – Spring 2014

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Outline

- Limits of Ultra-Low-Power Analog Circuit Design
- Limits of Ultra-Low-Voltage Analog Circuit Design
- MOS transistor in Weak Inversion
  - Definition
  - Properties
  - Impact of Short-Channel Effects on Weak Inversion
- Analog Circuits in Weak Inversion

Note: Contents of this Lecture are taken from a Short Course given in ISSCC 2012

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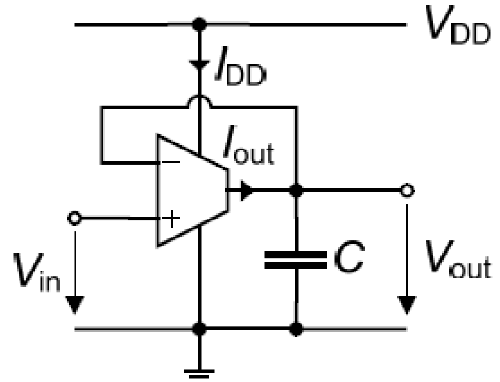
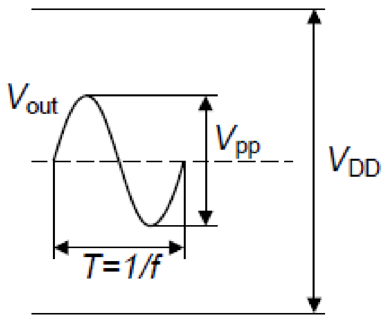
Limits of Ultra Low Power

- What are the fundamental **lower limits** to power consumption?





Assumptions:

100% efficient transconductor

(i.e. $I_{out}=I_{DD}$)

- Average value of I_{out}

$$\overline{I_{out}} = f \cdot C \cdot V_{pp}$$

- The **average power** consumption P is then given by

$$P = V_{DD} \cdot f \cdot C \cdot V_{pp} = \frac{V_{DD}}{V_{pp}} \cdot f \cdot C \cdot V_{pp}^2$$

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Limits to Ultra Low Power

- The **noise current** power spectral density (PSD) is given by

$$S_{Ni} = 4kT \cdot \gamma \cdot G_m$$

- The total mean square **noise voltage** across capacitor C is given by

$$V_N^2 = \frac{\gamma \cdot kT}{C}$$

- Where γ is the **noise excess factor** which will be assumed to be unity
- The **signal-to-noise** ratio SNR is then given by

$$SNR = \frac{V_{pp}^2/8}{kT/C} \quad \rightarrow \quad V_{pp}^2 = \frac{8kT}{C} \cdot SNR$$

- The **power consumption** can then be written as

$$P = 8 \cdot \frac{V_{DD}}{V_{pp}} \cdot kT \cdot f \cdot SNR$$

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Limits to Ultra Low Power

- Power consumption is minimized by maximizing the peak-to-peak signal with **rail-to-rail operation** $V_{pp}=V_{DD}$

$$P_{\min} = 8 \cdot kT \cdot f \cdot SNR$$

- P is proportional to frequency which actually corresponds to the **bandwidth B** for low-pass filters
- A factor of merit (actually demerit, the smaller the better) can be defined as

$$K = \frac{P}{kT \cdot B \cdot SNR} = 8 \cdot \frac{V_{DD}}{V_{pp}}$$

- K is **minimum** for $V_{pp}=V_{DD}$ (rail-to-rail linear operation)

$$K_{\min} = K\big|_{V_{pp}=V_{DD}} = 8$$

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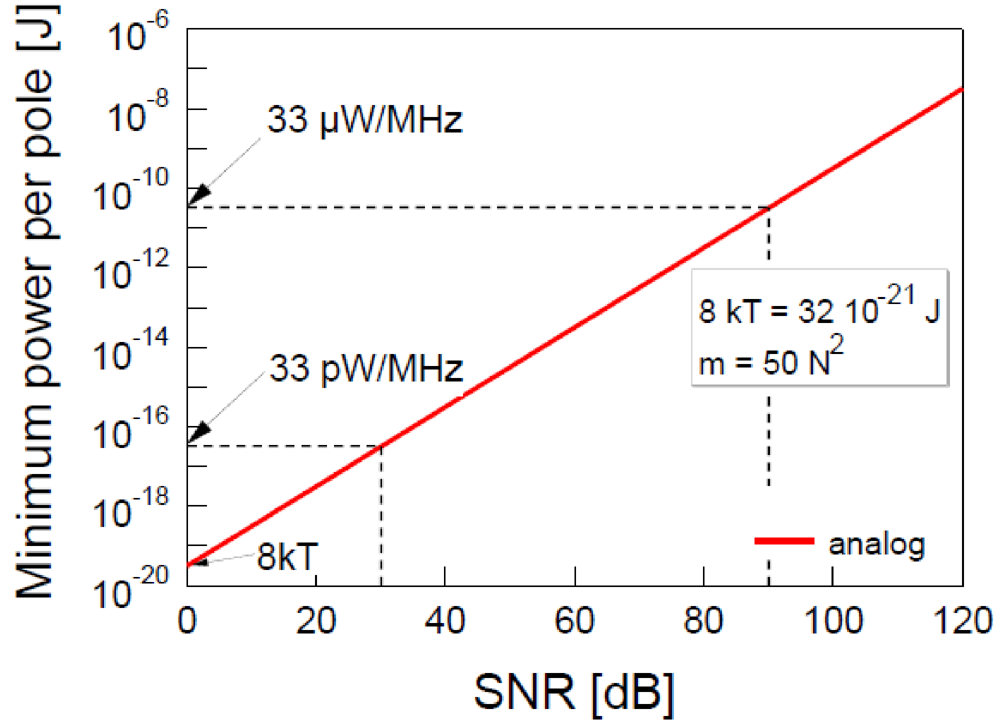
Min. Power Consumption versus SNR

- The **minimum** power consumption P_{min} is proportional to frequency (bandwidth)
- It corresponds to an **absolute minimum** for processing a signal with an analog circuit



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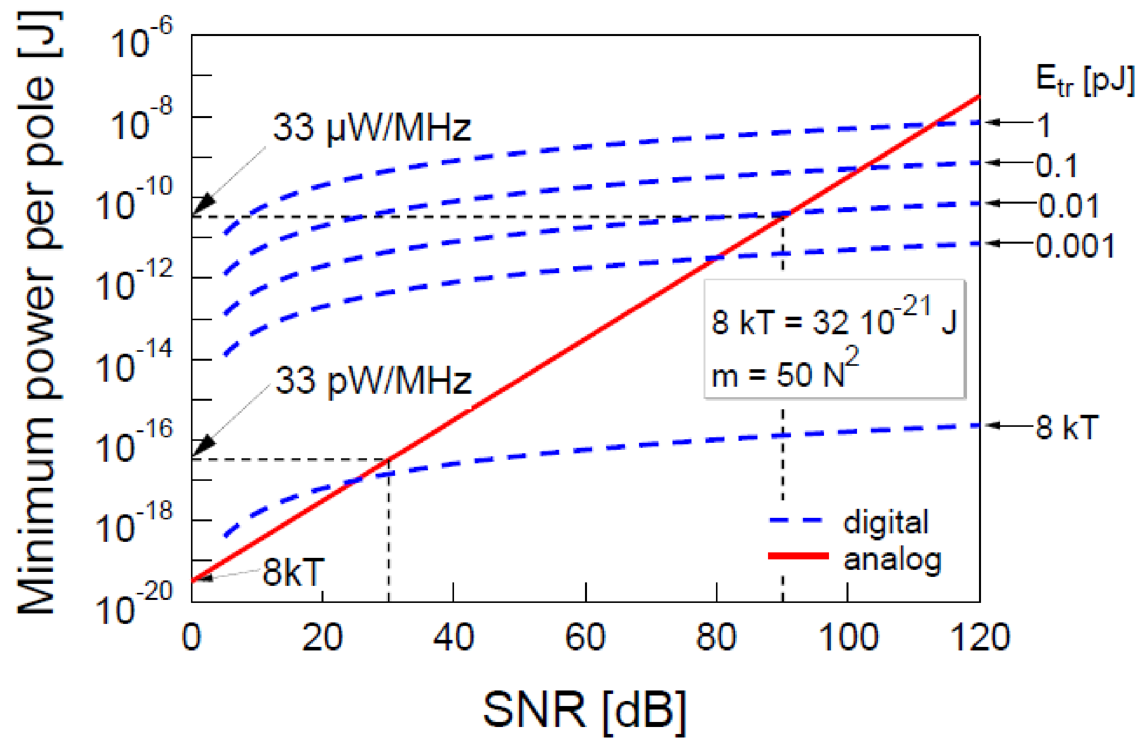
Min. Power Consumption versus SNR

- The **minimum** power consumption P_{min} is proportional to frequency (bandwidth)
- It corresponds to an **absolute minimum** for processing a signal with an analog circuit



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Practical Limits

- K_{min} constitute an **absolute minimum** not accounting for many non-idealities
- In practical analog circuits there are many **non-idealities** that can seriously degrade (increase) the K factor far beyond K_{min}
  - **Current inefficiency** (non-ideal class B operation)
  - **Linearity** requirement
  - Additional **bias** circuits
  - Limited **matching**
  - **Additional noise** contributions (from flicker noise and from other devices)
  - Parasitic **capacitances**
  - Charge injection

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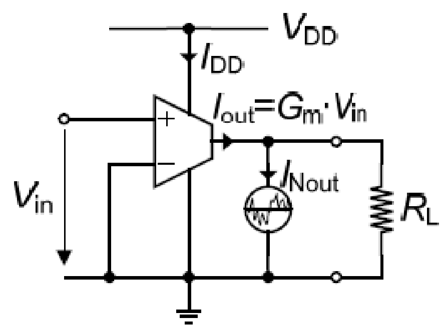
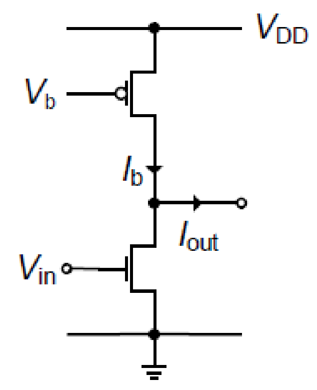
P_{min} for a Transconductance Amplifier



$$S_{I_{Nout}} = 4kT \cdot \gamma_{eq} \cdot G_m$$



$$V_{DD} > V_{DSsatn} + V_{DSsatp}$$

- K factor of a **generic transconductor** is given by

$$K = \frac{P}{kT \cdot B \cdot SNR} \geq 4\gamma_{eq} \frac{V_{DD} \cdot I_{DD}}{V_{in\text{-}rms}^2 \cdot G_m}$$

- Can be minimized by maximizing V_{in}/V_{DD} (rail-to-rail operation) and G_m/I_{DD} (bias in weak inversion)

- Example of a simple NMOS transconductor biased in SI for better linearity
- K minimum for $V_{DSsatn}=V_{DSsatp}=V_{DSsat}$

$$K > 8\gamma n \cdot \left(\frac{V_{DSsat}}{V_{in\text{-}rms}} \right)^2$$

- Can be minimized by reducing V_{DSsat} and hence the supply voltage V_{DD}

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P_{min} for a Transconductance Amplifier

- However, decreasing V_{DSsat} increases the **total harmonic distortion** THD due to the square-law characteristic according to

$$THD = \frac{V_{in}}{4nV_{DSsat}} = \frac{\sqrt{2} \cdot V_{in\text{-}rms}}{4nV_{DSsat}} \quad \rightarrow \quad \left(\frac{V_{DSsat}}{V_{in\text{-}rms}}\right)^2 = \frac{1}{8n^2 \cdot THD^2}$$

- K can then be expressed directly in terms of the THD as

$$K > \frac{\gamma}{THD^2} = \frac{2}{3 \cdot THD^2}$$

- Having THD < 1% requires K > 6700 instead of 8 (**factor 840 higher!**)

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Why Low Voltage?

- Two main motivations for low-voltage:
  1. Reduce the **dynamic power consumption** of digital circuits according to

$$P_{dyn} = f \cdot C \cdot V_{DD}^2$$

  2. Maintaining limited electric field in the device and avoid strong short-channel effects due to **process down-scaling**
- But definitely **NOT** to reduce the power consumption of **analog circuits**
- Low-voltage usually results in **higher power consumption** for analog circuits
- Low-voltage is often imposed the full **system integration** (system-on-a-chip or SoC approach) including analog and RF in deep-submicron technologies
- Low-voltage can also be imposed by **energy-scavenging** sources producing only small supply voltages

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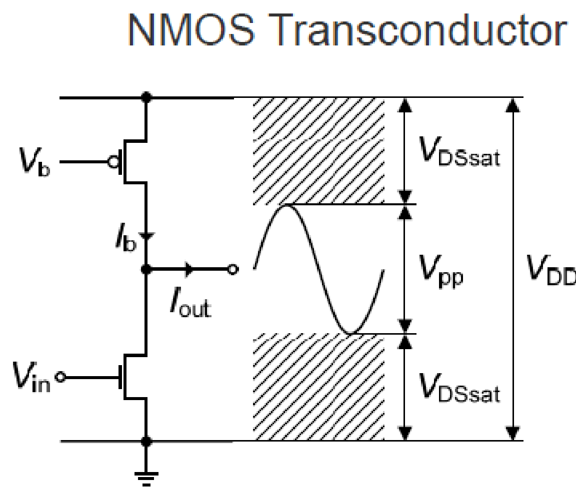
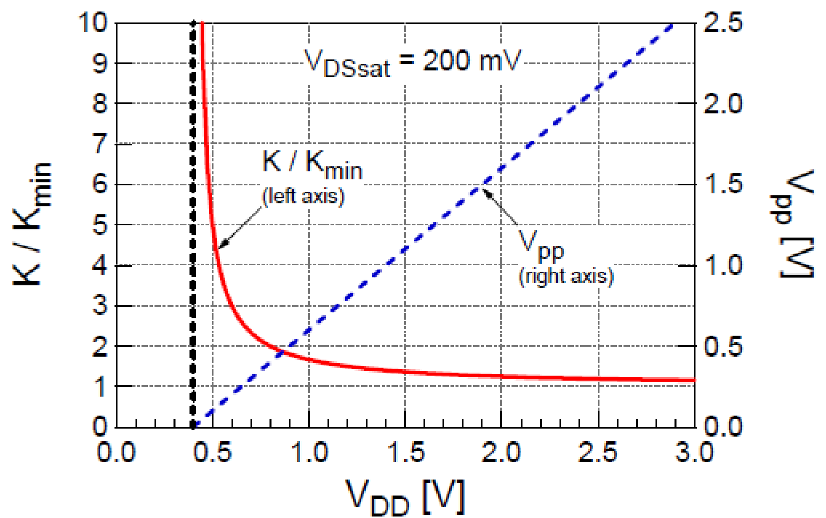
Impact of Supply Voltage Reduction on Power Consumption





- Assuming **uncompressible** and **equal saturation voltages** for NMOS and PMOS, the minimum supply voltage for a given signal voltage swing is given by

$$V_{DD} = V_{pp} + 2V_{DSsat} \quad \rightarrow \quad V_{pp} = V_{DD} - 2V_{DSsat}$$

- The power consumption is now given by

$$P = K_{\min} \cdot \frac{V_{DD}}{V_{DD} - 2V_{DSsat}} \cdot kT \cdot B \cdot SNR \quad \text{or} \quad \frac{K}{K_{\min}} = \frac{V_{DD}}{V_{DD} - 2V_{DSsat}}$$

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Consequences of Supply Voltage Reduction

- Most fundamental
  - Voltage swing given by $V_{pp} \leq V_{DD} - 2 \cdot V_{DSsat}$
  - If $V_{DSsat} = V_{DD}/2$ (or $V_{pp} = 0$) then K >>> 1
  - If voltage is split half between bias and signal: $V_{DSsat} = V_{DD}/4$ (or $V_{pp} = V_{DD}/2$) then K acceptable
- V_{pp} and V_{DSsat} **must therefore be reduced proportionally with V_{DD}** , consequently, inversion coefficient has to be reduced and **operating point is progressively moving towards moderate and weak inversion**
- Other consequences:
  - V_{DD} approaching V_T → poor switch conductance (eventually conductance gap)
  - If V_T is lowered → open switches start to leak
  - V_{DD} below V_{G0} → requires special band-gap voltage reference circuits
  - Transistor stacks no more possible → requires special LV circuit techniques

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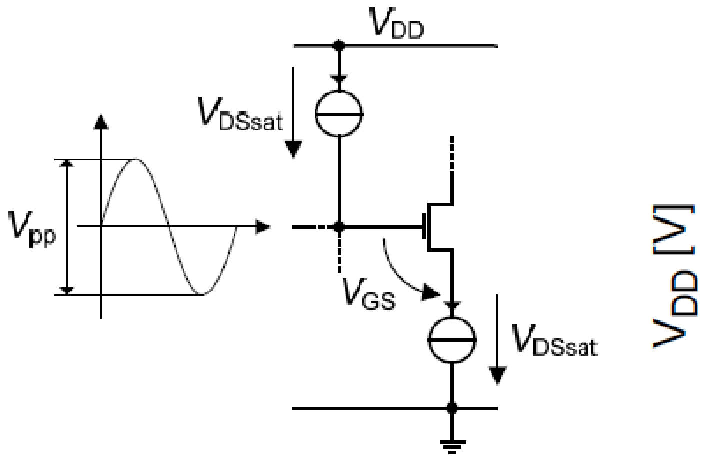
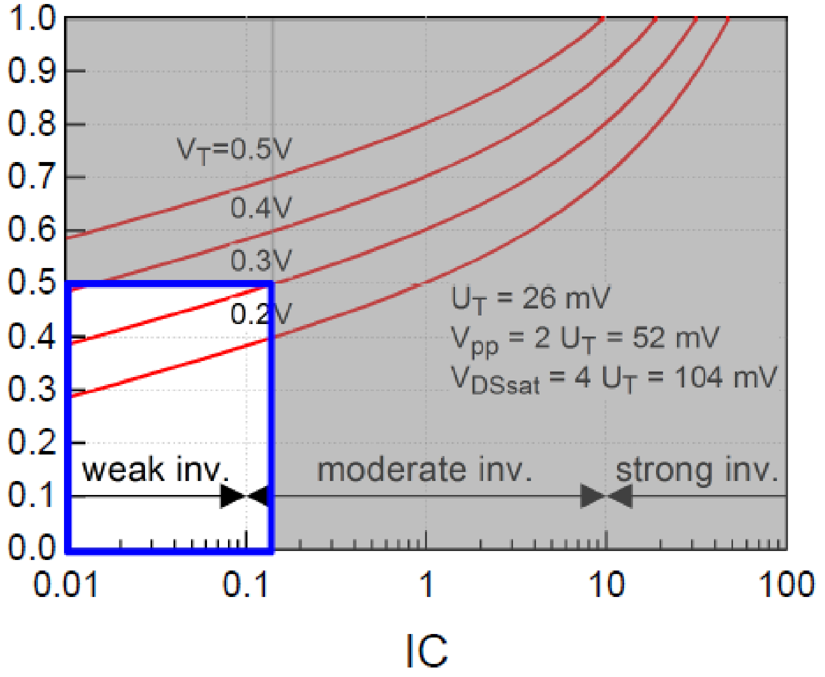
Minimum Supply in Weak Inversion for Different V_T





$$V_{DD} = V_{GS} + 2V_{DSsat} + V_{pp}$$

$$V_{GS} = V_T + 2n \cdot U_T \cdot \ln\left(e^{\sqrt{IC}} - 1\right)$$

- Supply voltage below 1V **pushes bias point towards moderate/weak inversion**
- For achieving V_{DD}=0.5V, threshold voltage should be smaller than 0.3 V and bias point has to be in weak inversion (IC < 0.1)

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MOSFET Models

Bulk MOSFET Models

- BSIM3
  - Threshold Voltage based MOSFET Model
  - First CMC standard Model
- BSIM4
  - Threshold Voltage based MOSFET Model with enhanced physics features (mobility, BTBT, gate leakage…..)

- BSIM6
  - Charge based Symmetric MOSFET Model
    - Charge based core
    - BSIM4 physics models and parameters
  - Under standardization review in CMC

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45-min Seminar [1]

- BSIM6 Model description (EKV)
- Why use Charge-based Models?
- Background on Charge Based Symmetric Model
- Charge, Current and Voltage Expressions in more details
- All transconductances expressions
- Special Cases
- Important Derivations

[REF1] C. C. Enz and E. A. Vittoz, *Charge-Based MOS Transistor Modeling - The EKV Model for Low-Power and RF IC Design*, John Wiley, 2006.

[REF2] E. A. Vittoz and C. C. Enz, "EKV Model of the MOS Transistor," in *Sub-Threshold Design for Ultra Low-Power Systems*, Springer, 2006.

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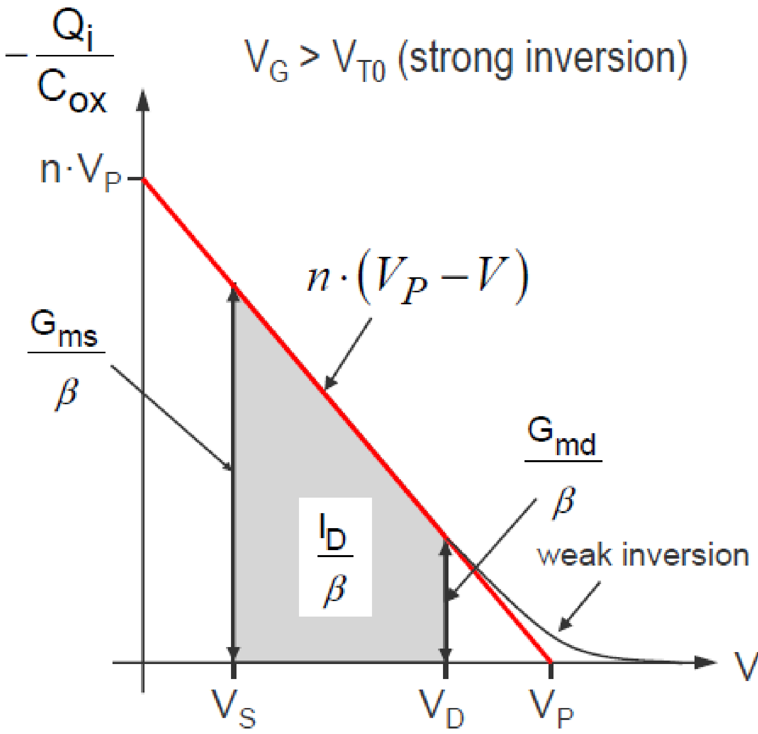
Drain Current

$$I_D = \mu \cdot W \cdot (-Q_i) \cdot \frac{dV}{dx} \quad \Rightarrow \quad I_D = \beta \cdot \int_{V_S}^{V_D} \frac{-Q_i}{C_{ox}} \cdot dV \quad \text{with} \quad \beta = \mu \cdot C_{ox} \cdot \frac{W}{L}$$



- Q_i is the inversion mobile charge density (electrons for n-channel)
- V is the **channel voltage** (electrons quasi-Fermi potential), equal to V_S at the source and V_D at the drain
- V_P is the **pinch-off voltage** given by

$$V_P \cong \frac{V_G - V_{T0}}{n}$$

- V_{T0} is the **threshold voltage** (at V=0)
- n is the **slope factor**
- μ is the electron mobility (at low field)

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Charge-Based Forward and Reverse Currents

- $I_D = I_F - I_R$
- Normalized drain current (Inversion Coefficient - IC):
  - $i_d = i_f - i_r = (\mathrm{q_s^2} + \mathrm{q_s}) - (\mathrm{q_d^2} + \mathrm{q_d})$
  - $\mathrm{q_s}$: Normalized charge density in the channel near the source
  - $\mathrm{q_d}$: Normalized charge density in the channel near the drain

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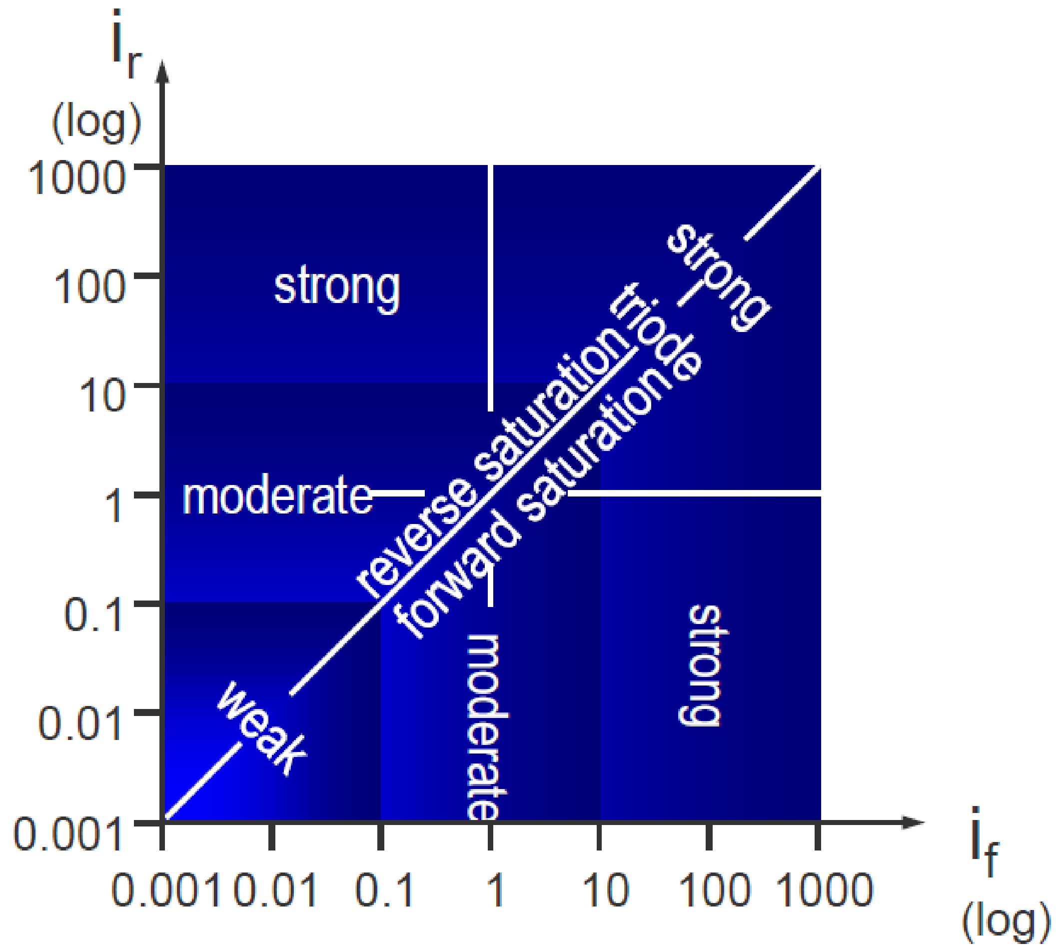
Modes of Operation (i_f $versus$ i_r)



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Approximate Current Expression (Valid in all regions)

$$i_{f(r)} = \frac{I_{F(R)}}{I_{spec}} = \ln^2\left(1 + e^{\frac{V_P - V_{S(D)}}{2U_T}}\right) \cong \ln^2\left(1 + e^{\frac{V_G - V_{T0} - n \cdot V_{S(D)}}{2n \cdot U_T}}\right)$$

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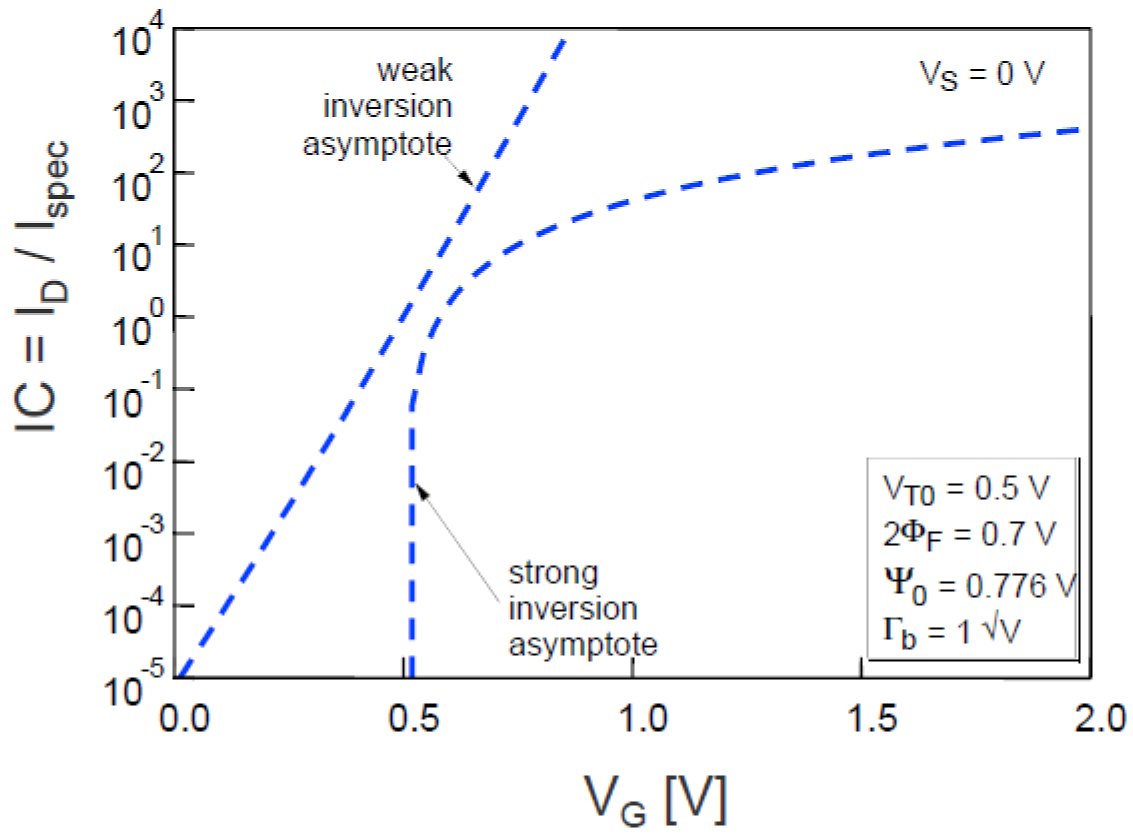
Moderate and Weak Inversion



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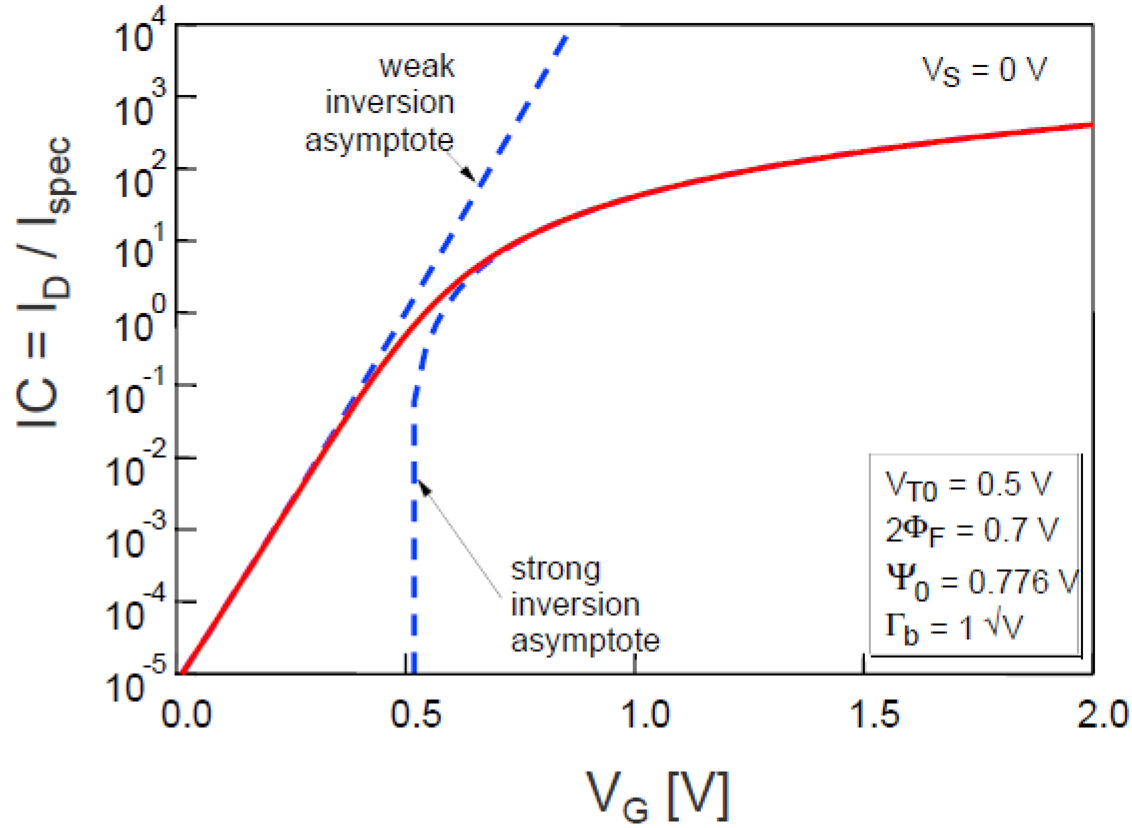
Moderate and Weak Inversion



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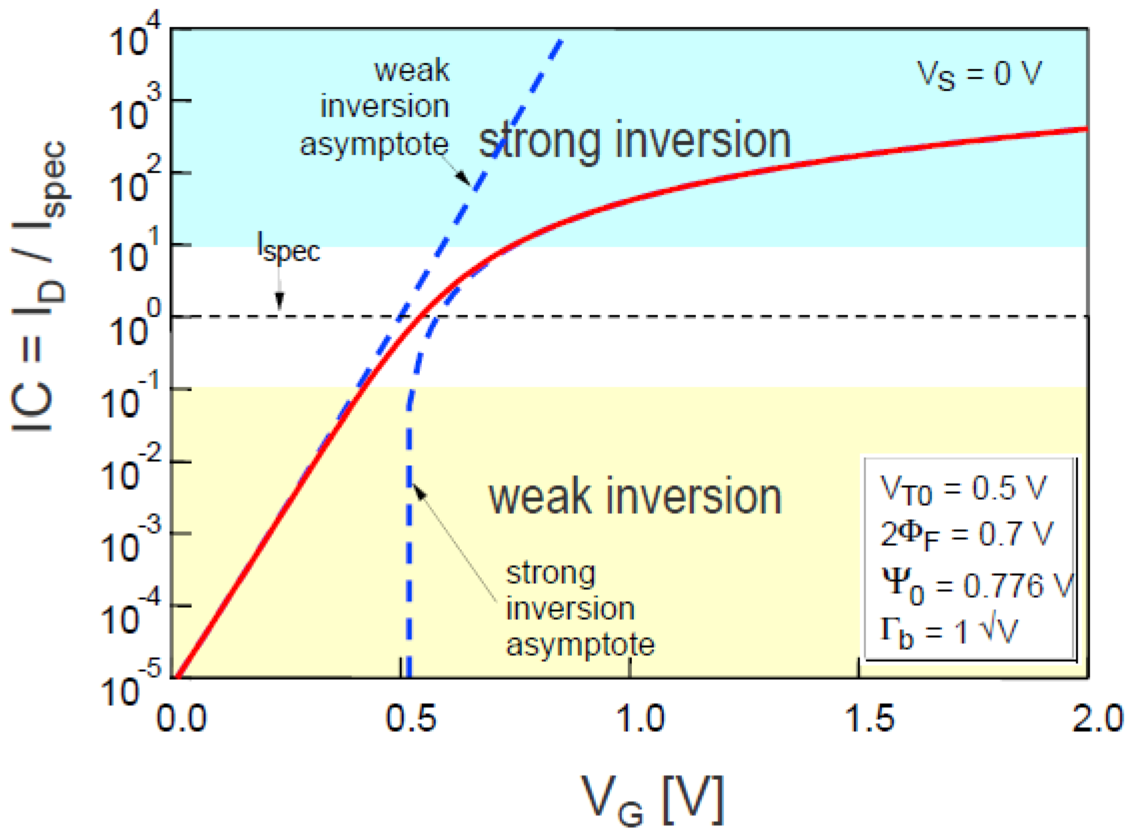
Moderate and Weak Inversion



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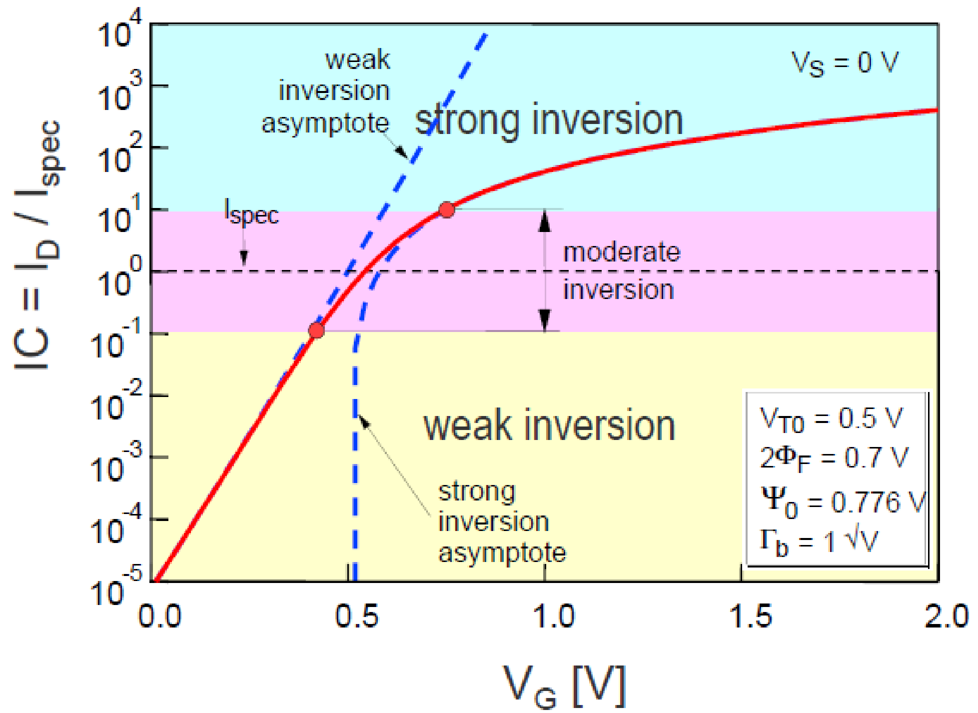
Moderate and Weak Inversion



- Strong inversion spans over wide range of voltage, but…
- **Moderate** and **weak inversion** span over **more than 6 decades of current**, whereas strong inversion is limited to less than 2 decades

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Drain Current in Weak Inversion

- Drain current in **weak inversion**

$$I_D = I_F - I_R = I_{spec} \cdot \left(i_f - i_r\right) \quad \text{with} \quad I_{F(R)} = I_{spec} \cdot e^{\frac{V_P - V_{S(D)}}{U_T}}$$

where I_F (i_f) and I_R (i_r) are the **forward** and **reverse** (normalized) currents, respectively and I_{spec} is the **specific current** defined by

$$I_{spec} = 2n \cdot \beta \cdot U_T^2 = I_{spec\square} \cdot \frac{W}{L}$$

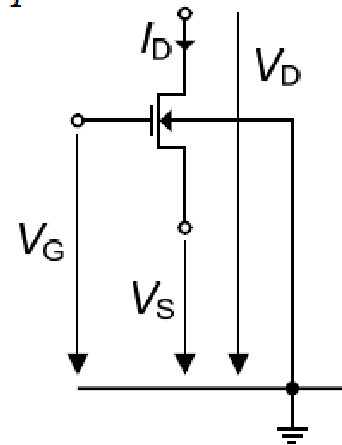
$$\text{with} \quad \beta = \mu \cdot C_{ox} \cdot \frac{W}{L} \quad \text{and} \quad I_{spec\square} = 2n \cdot \mu \cdot C_{ox} \cdot U_T^2$$

- V_P is the **pinch-off voltage** given by

$$V_P = \frac{V_G - V_{T0}}{n}$$

- The drain current can then be written as

$$I_D = I_{spec} \cdot e^{\frac{V_G - V_{T0}}{n \cdot U_T}} \cdot \left[e^{-\frac{V_S}{U_T}} - e^{-\frac{V_D}{U_T}} \right]$$



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Drain Current in Weak Inversion

- The drain current can also be written as

$$I_D = I_F \cdot \left(1 - \frac{I_R}{I_F}\right) = I_F \cdot \left(1 - e^{-\frac{V_{DS}}{U_T}}\right)$$

- **Saturation** is reached for $V_{DS} >> U_T$

$$I_D = I_F = I_{spec} \cdot e^{\frac{V_P - V_S}{U_T}} = I_{spec} \cdot e^{\frac{V_G - V_{T0} - n \cdot V_S}{n U_T}} = I_{D0} \cdot e^{\frac{V_G - n \cdot V_S}{n U_T}}$$

where I_{D0} is the **leakage current** (current flowing in saturation for $V_G=V_S=0$)

$$I_{D0} = I_{spec} \cdot e^{-\frac{V_{T0}}{n \cdot U_T}}$$

- Leakage current **highly sensitive to threshold voltage**

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Drain Current in Saturation versus VGS

- The saturation voltage $V_P - V_S$ can be expressed in terms of the V_{GS} voltage as

$$V_P - V_S \cong \frac{V_G - V_{T0} - n \cdot V_S}{n} = \frac{V_{GS} - V_T}{n}$$

where V_T is the threshold voltage for $V_S > 0$

$$V_T = V_{T0} + (n-1) \cdot V_S$$

- The drain current in **forward saturation** (forward current) can then be written in terms of the V_{GS} voltage as

$$i_d = \frac{I_D}{I_{spec}} \cong i_f \cong \ln^2\left(1 + e^{\frac{V_{GS} - V_T}{2n \cdot U_T}}\right)$$

- Which in **weak inversion** and **forward saturation** reduces to

$$i_d = \frac{I_D}{I_{spec}} \cong \cdot e^{\frac{V_{GS} - V_T}{nU_T}}$$

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Inversion Coefficient

- Overdrive voltage $V_{GS}-V_T$ not convenient for weak inversion
- Replaced by the **inversion coefficient IC** characterizing the global level of inversion of the transistor and formerly defined as

$$IC = \max\left(i_f, i_r\right)$$

- In **saturation** $i_f >> i_r$ and therefore

$$IC = i_f = \frac{I_D}{I_{spec}} = \frac{I_D}{I_{spec\square} \cdot \frac{W}{L}} \quad \text{(saturation)} \quad \text{with} \quad I_{spec\square} = 2n \cdot \mu \cdot C_{ox} \cdot U_T^2$$

- The different regions of operation in **saturation** can then be defined as

IC < 0.1:	**weak** inversion (WI)
0.1 < IC < 10:	**moderate** inversion (MI)
10 < IC:	**strong** inversion (SI)

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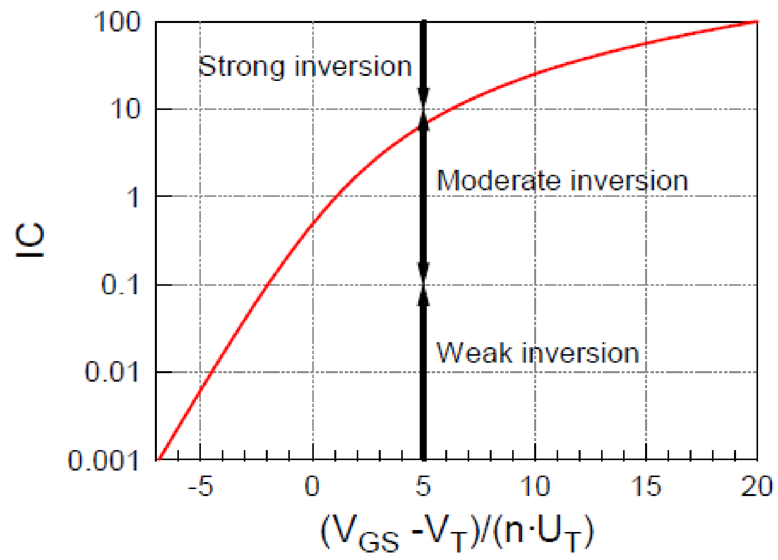
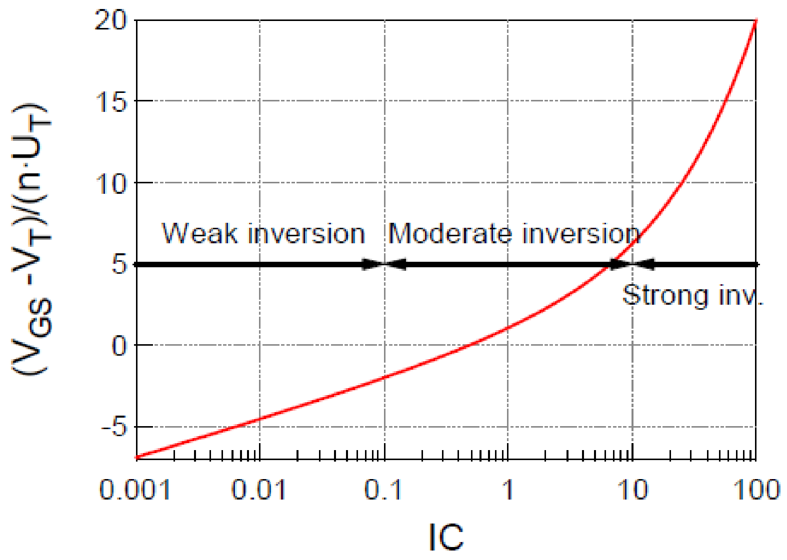
IC versus Overdrive Voltage

- The inversion coefficient IC (in saturation) can be expressed in terms of the overdrive voltage $V_{GS}-V_T$ and reversely

$$IC = \frac{I_D}{I_{spec}} = \ln^2\left(1+e^{\frac{V_{GS}-V_T}{2n \cdot U_T}}\right)$$

$$\frac{V_{GS}-V_T}{n \cdot U_T} = 2 \cdot \ln\left(e^{\sqrt{IC}}-1\right)$$





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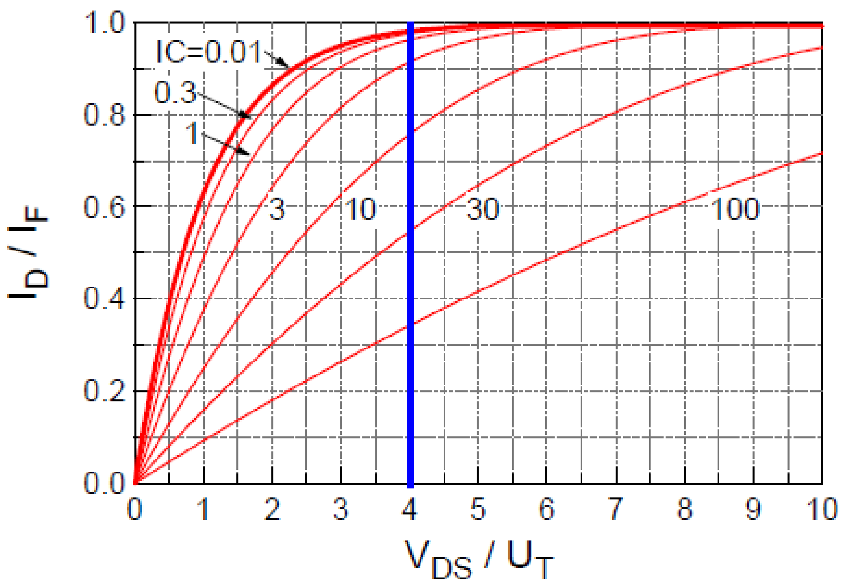
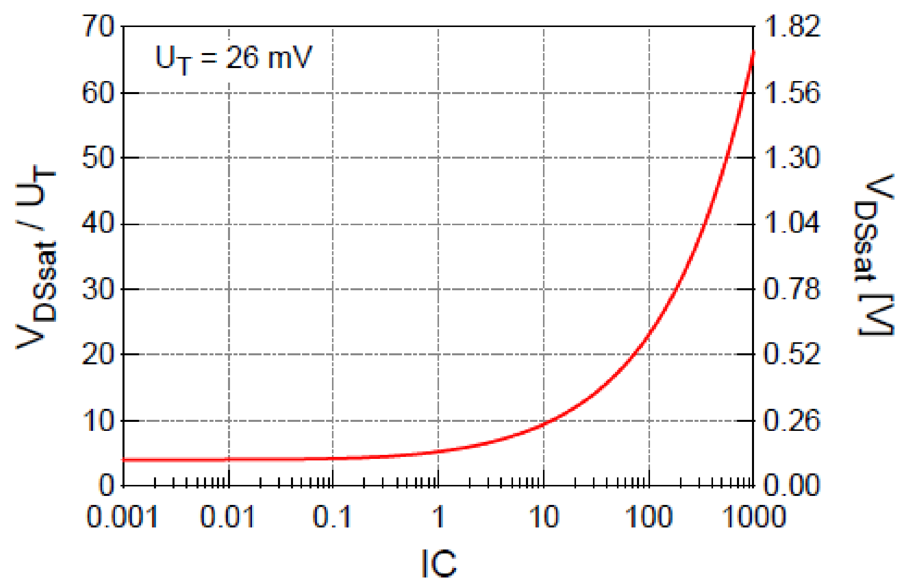
[1] Lowest Saturation Voltage





$V_{DSsat} \approx 4\ UT \approx 100$ mV

- Weak inversion provides the **minimum saturation voltage** ($V_{DSsat} \cong 4$ to $5\ U_T$)
- This is the main reason why weak inversion is intrinsically associated with **low-voltage circuit design**
- Unlike strong inversion, this saturation voltage is **independent of the threshold voltage**

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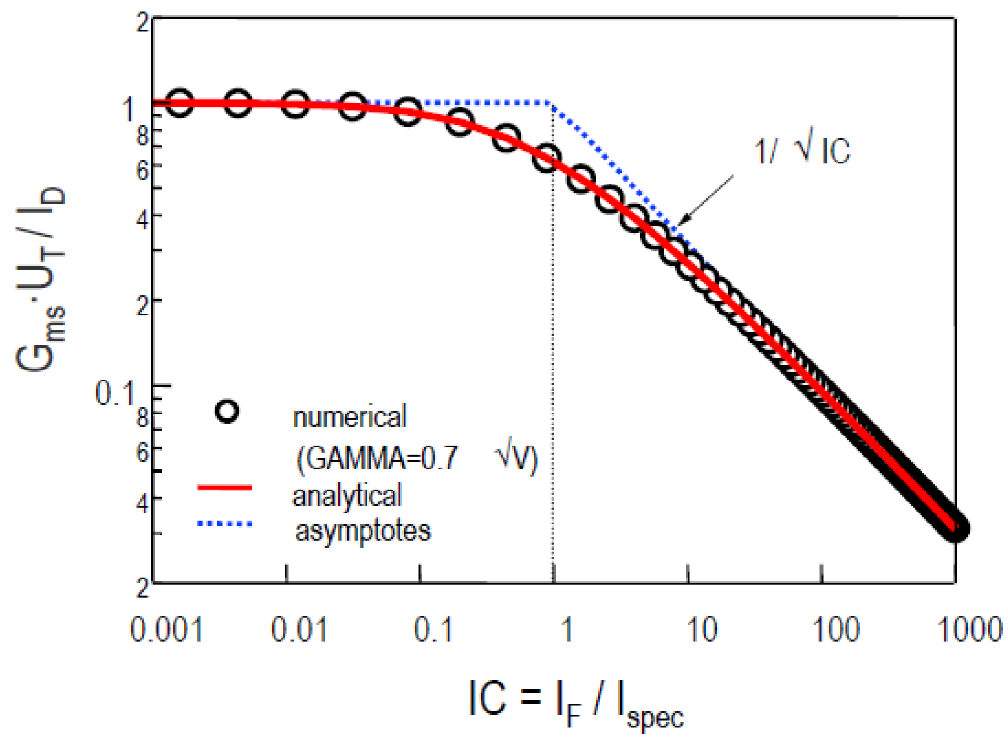
[2] Maximum Current Efficiency (G_m/I_D)

- The **current efficiency** (in saturation) is maximum in weak inversion

$$\text{current efficiency} = \frac{G_{ms} \cdot U_T}{I_D} = \frac{G_m \cdot n \cdot U_T}{I_D} = \frac{1}{q_s + 1} == \frac{2}{\sqrt{4IC+1}+1} = \begin{cases} 1 & WI \\ 1/\sqrt{IC} & SI \end{cases}$$



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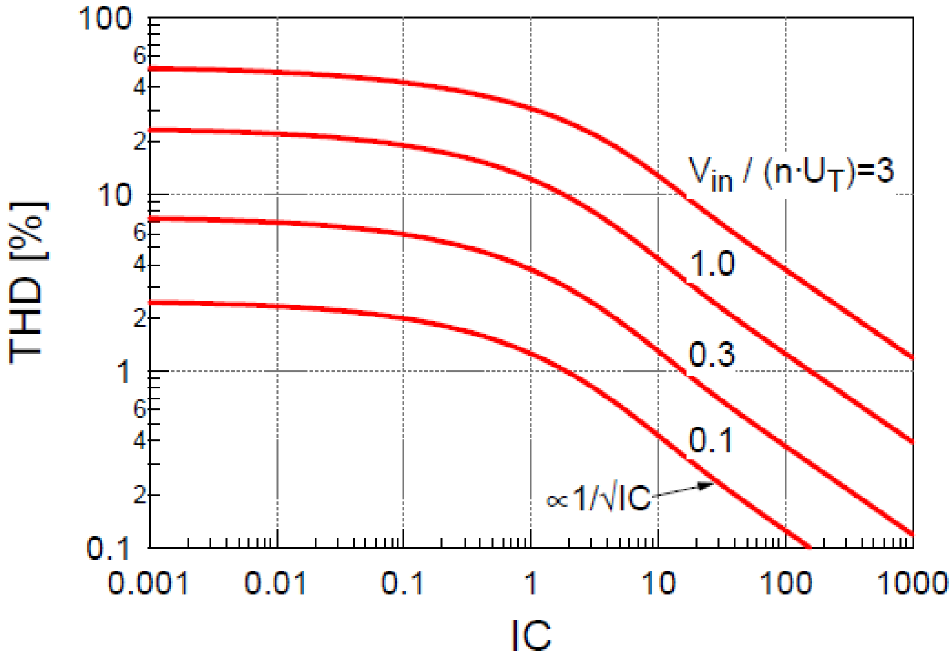
[3] THD of Drain Current versus IC



Fourier coefficients in WI:

$$a_0 = \frac{I_{D(0)}}{I_{spec}} = IC \cdot \mathrm{I}_{B0}(x)$$

$$a_n = \frac{I_{D(n)}}{I_{spec}} = 2IC \cdot \mathrm{I}_{Bn}(x)$$

where I_{Bn} are the modified Bessel function of the 1st-kind of order n

- Above plot shows the THD in % versus the inversion factor for different sinewave input amplitudes
- **Linearity** is strongly **degraded** compared to SI due to the exponential I-V characteristic

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[4] Matching

- Assuming ΔV_{T0} and $\Delta\beta$ are uncorrelated and Δn is negligible, the standard deviation of the **relative drain current mismatch** of two transistors biased in **saturation** with the same gate and source voltages (current mirror) is given by

$$\sigma_{\frac{\Delta I_D}{I_D}} = \sqrt{\sigma^2_{\frac{\Delta\beta}{\beta}} + \left(\frac{G_m}{I_D}\right)^2 \cdot \sigma^2_{\Delta V_{T0}}}$$

with $\sigma_{\frac{\Delta\beta}{\beta}} = \frac{A_\beta}{\sqrt{W \cdot L}}$ and $\sigma_{\Delta V_{T0}} = \frac{A_{VT}}{\sqrt{W \cdot L}}$ with $A_{VT} \propto t_{ox} \cdot \sqrt[4]{N_b} \propto \frac{\sqrt[4]{\kappa}}{\kappa} = \frac{1}{\kappa^{3/4}}$

- The standard deviation of the **gate voltage mismatch** of two transistors biased in **saturation** with identical drain current (diff pair) is given by

$$\sigma_{\Delta V_G} = \sqrt{\sigma^2_{\Delta V_{T0}} + \left(\frac{I_D}{G_m}\right)^2 \cdot \sigma^2_{\frac{\Delta\beta}{\beta}}}$$

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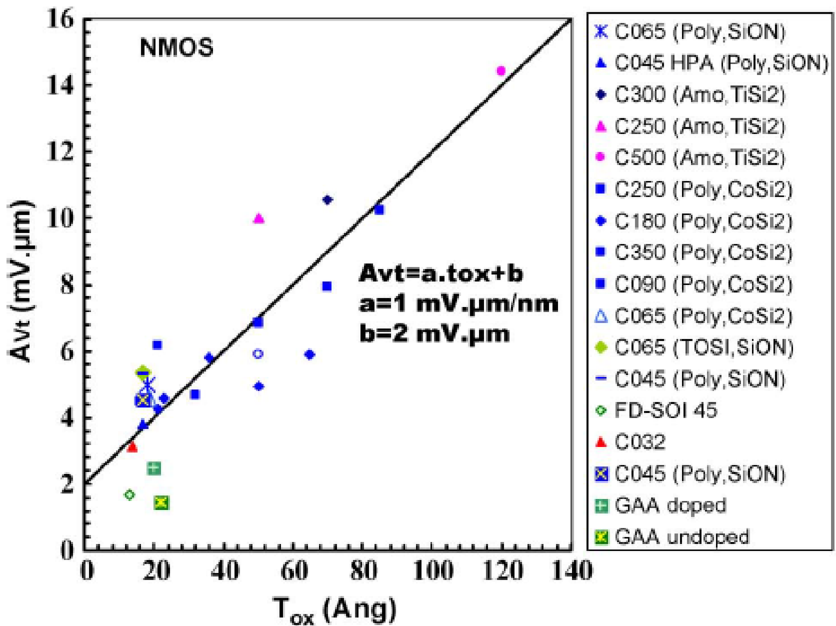
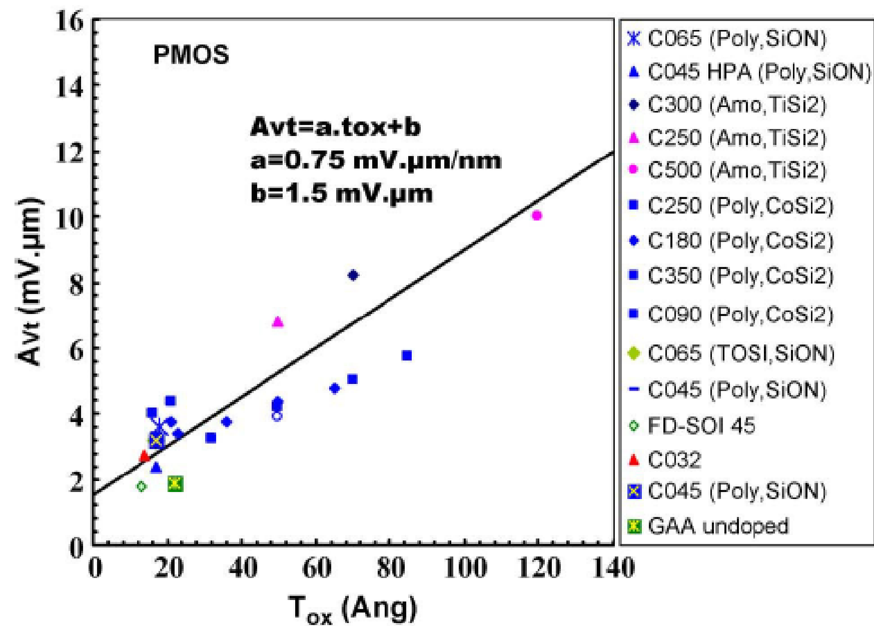
[4] Matching – Downscaling improves Matching

$$A_{VT} \propto t_{ox} \cdot \sqrt[4]{N_b} \propto \frac{\sqrt[4]{\kappa}}{\kappa} = \frac{1}{\kappa^{3/4}}$$ where κ is the scaling factor





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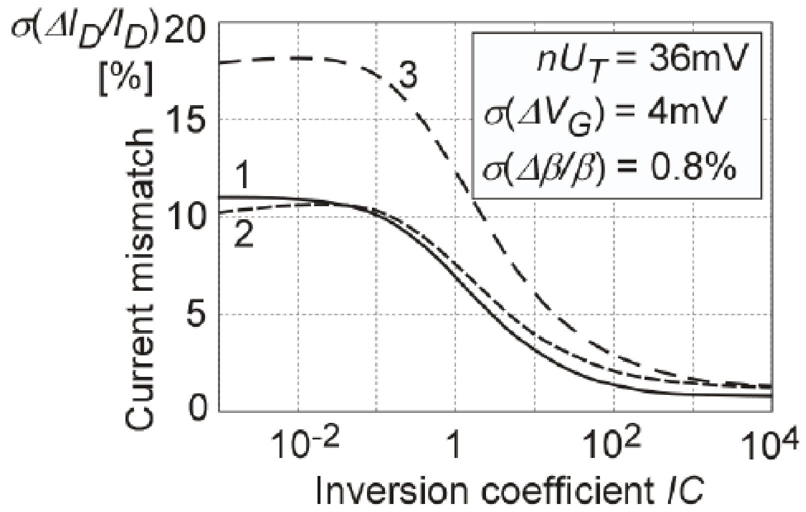
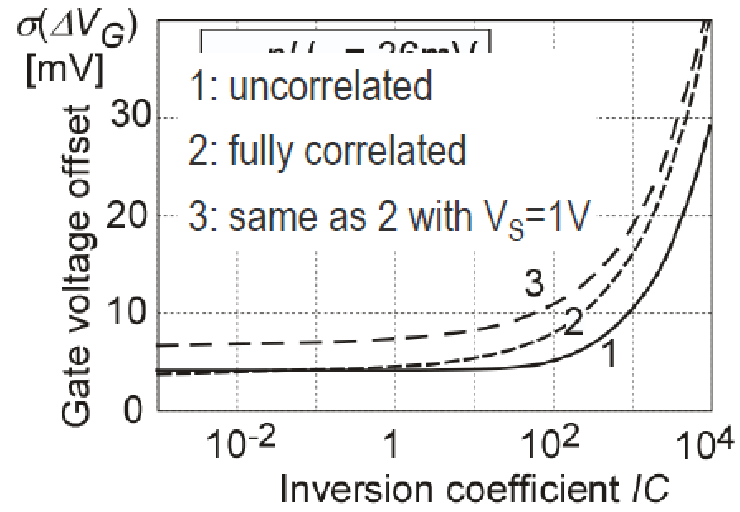
[4] Matching





- Current matching bad in weak inversion
- Gate voltage matching best in weak inversion
- Nonzero V_S degrades matching, (particularly current matching in WI) due to correlation between ΔV_{T0} and Δn (both depend on doping variation ΔN_b)

$$\sigma_{\Delta V_T}\Big|_{V_S>0} = \sigma_{\Delta V_{T0}} \cdot \left(1 + \frac{V_S}{2\Psi_0}\right)$$

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[5] Limiting the Speed (Bandwidth)

- The transit frequency in WI and saturation is given by

$$\omega_t = \frac{G_m}{C_G} = \frac{G_m}{C_{Gi} + C_{Ge}} \cong \omega_{t0} \cdot IC$$

where C_G is the **total gate capacitance** made of the intrinsic C_{Gi} and extrinsic C_{Ge} gate capacitances respectively, and ω_{t0} is defined as the ω_t (in WI) for IC=1

- **Proportional to inversion coefficient** (instead of $\sqrt{IC}$ in SI)
- Takes full advantage of $1/L^2$ scaling since there is no high field effects such as velocity saturation and mobility reduction due to the vertical field
- Extrinsic capacitances (overlap and fringing capacitances) strongly reduce the f_t (typically a factor 3 compared to intrinsic f_t)
- For typical 65 nm process $f_{t0} \cong 300$ GHz for n-channel MOST (standard V_T)

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Summary of Properties

Pros

- Exponential I-V characteristic similar to bipolar
- Minimum drain saturation voltage
- Minimum gate voltage
- Minimum gate capacitance
- Maximum current efficiency G_m/I_D
  - Max. intrinsic voltage gain
  - Min. input noise PSD for given I_D
  - Max. bandwidth for given kT/C and I_D
  - Min. input offset voltage

Cons

- Higher distortion
- Low speed
- Low f_t compared to strong inversion, but increases with scaling (weak inversion is more and more interesting for deep-submicron technologies)
  - Max. output noise current for a given I_D
  - Max. current mismatch (poor current accuracy)

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Outline

- **Limits of Ultra-Low-Power Analog Circuit Design**
- **Limits of Ultra-Low-Voltage Analog Circuit Design**
- **MOS transistor in Weak Inversion**
  - **Definition**
  - **Properties**
  - Impact of Short-Channel Effects on Weak Inversion

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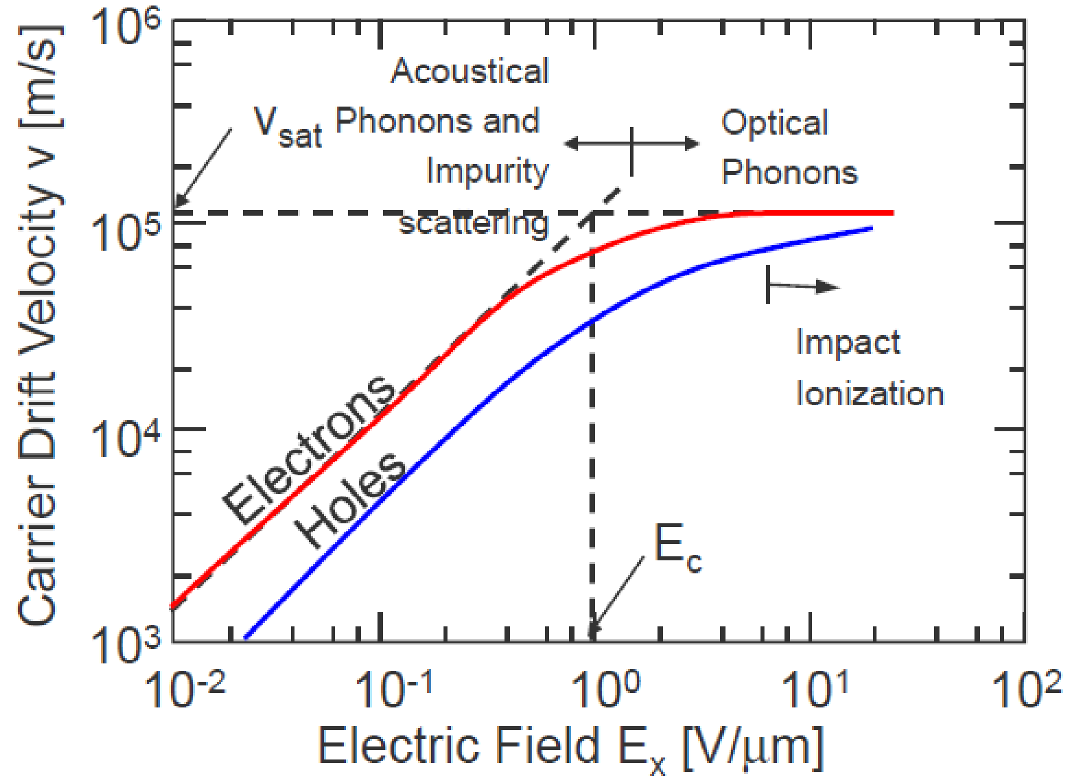
Velocity Saturation

- A high longitudinal electric field E_x causes the carrier velocity v_{drift} to saturate



For Si

Electrons:

$v_{sat} \cong 10^5$ m/s

$E_c \cong 1$ V/µm

Holes:

$v_{sat} \cong 8 \times 10^4$ m/s

$E_c \cong 3$ V/µm

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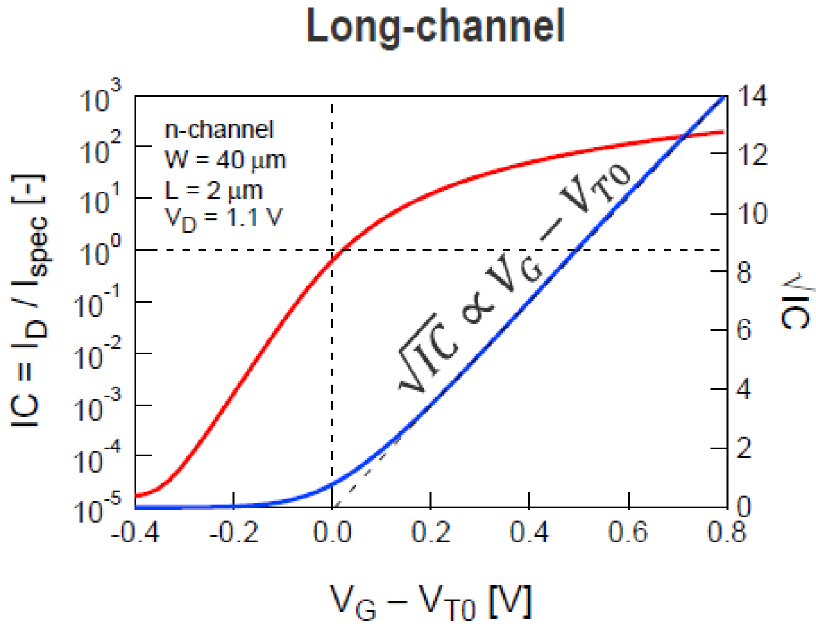
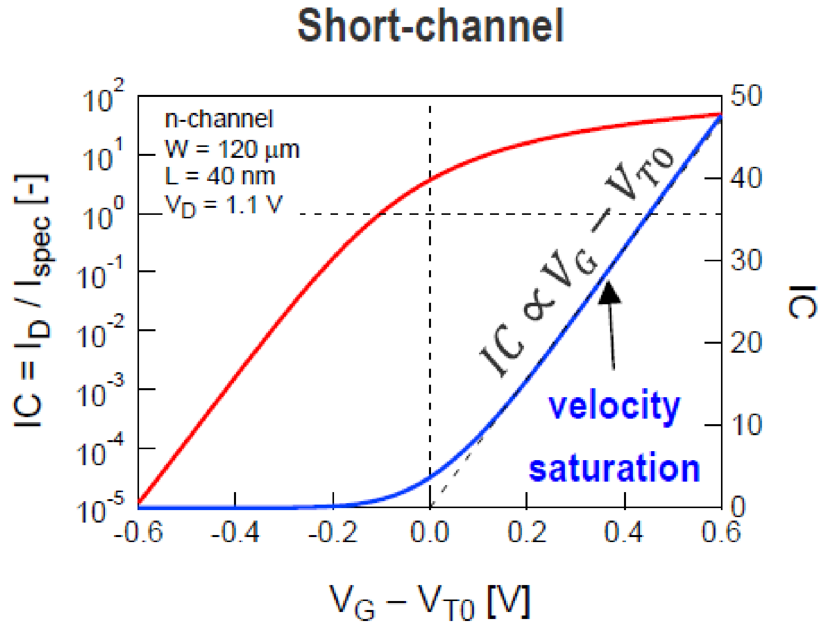
Effect of Velocity Saturation on Drain Current





- Velocity saturation has a strong impact on the drain current in strong inversion
- The current becomes proportionnal to $V_G - V_{T0}$
- Hence the gate and source transconductances become independent of the current (and independent of the length)

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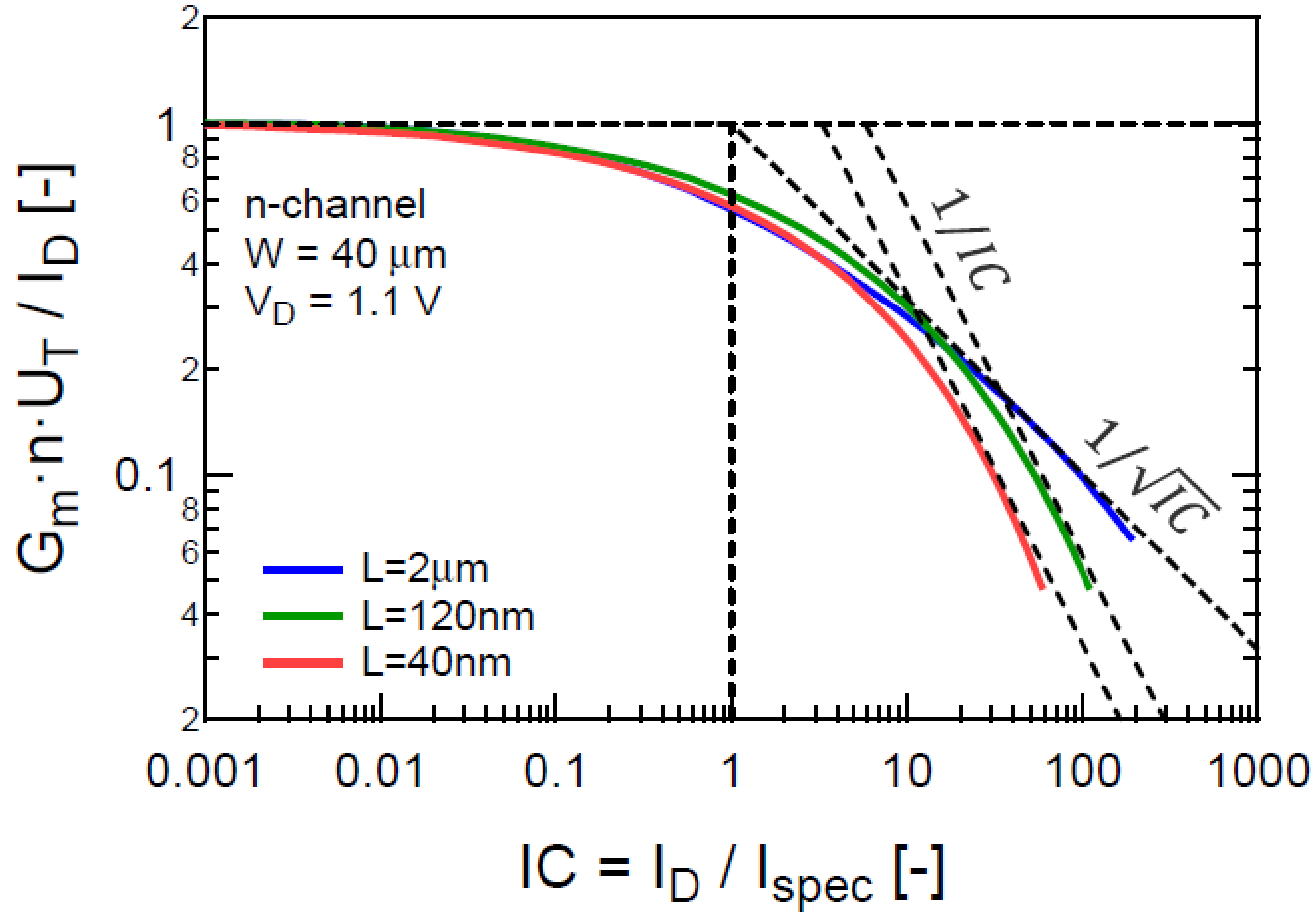
Effect of Velocity Saturation on Current Efficiency



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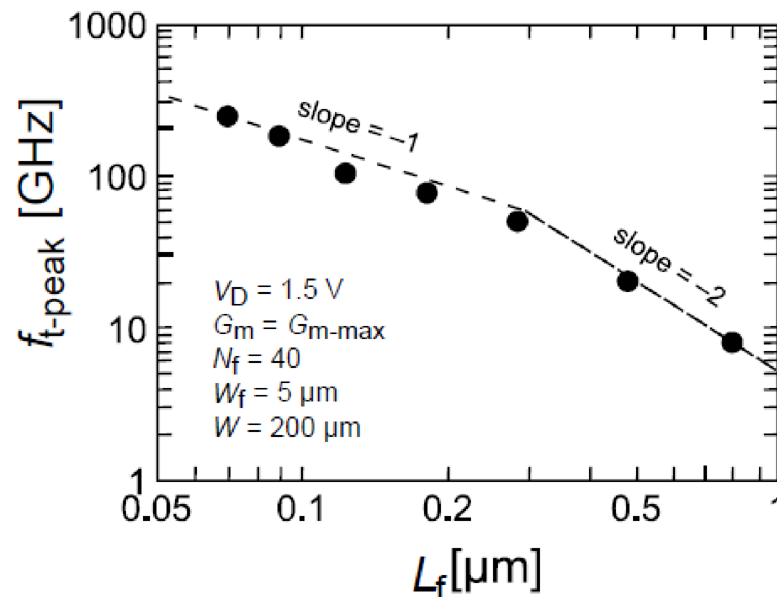
Transit Frequency Scaling

- Scaling of ω_t is affected by short-channel effects such as **velocity saturation**

$$\left.\begin{aligned} G_{msat} &\cong W \cdot C_{ox} \cdot v_{sat} \\ C_G &\propto W \cdot L_f \cdot C_{ox} \end{aligned}\right\} \rightarrow \omega_t = \frac{G_{msat}}{C_G} \propto \frac{v_{sat}}{L_f}$$

- Scales only as $1/L_f$ instead of $1/L_f^2$ when velocity saturation is present



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